Migrating From EZ-USB FX2™ to EZ-USB FX2LP™

Abstract

The FX2LP is a next-generation USB high-speed controller. FX2LP enhances the functionality of the FX2 while minimizing the effects on existing designs. The purpose of this application note is to expedite the developer's learning curve regarding the migration of a CY7C68013 (EZ-USB FX2™) design to use the CY7C68013A (EZ-USB FX2LP™) microcontrollers. This application note highlights the difference between the two products and aids the designer in migrating existing designs to FX2LP. The application note also provides a brief description of the collateral available for development work with FX2LP.

Hardware Changes

Changes on Crystal Specification

With the use of FX2LP one change is required. When a crystal is used in the design, for proper operation the load capacitance of the crystal is required to change. This effects both the load capacitors and the crystal being used. The CY7C68013 requires a crystal with load capacitors that are between 20 pF and 33 pF. The CY7C68013A requires a crystal with load capacitors of 12 pF. If redesigning an FX2 application with FX2LP, the crystal is required to change to a load capacitance of 12 pF, and the matching load capacitors must change to 12 pF. This is a requirement of all designs using FX2LP.

Following is the spec on the crystal

- 24 MHz $\pm$100 ppm
- Parallel resonant
- Fundamental mode
- 500 μW drive level
- 12-pF (5% tolerance) load cap

One of the parts we recommend is one from Ecliptek: EC-12-24.000M

The above specification must betaken into consideration while selecting both the load capacitors and the crystal. Using a different crystal load capacitance with a crystal specified for 12 pF is expected to have some effect on the frequency shift. It is recommended that the designer always make sure that the power dissipated by the crystal is with-in the crystal manufacturer's specifications. Over-driving the crystal may damage the crystal. Refer to the specific crystal manufacturer's recommendations.

An article on crystal design and selection from *Ecliptek's* site (http://www.ecliptek.com/crystals/glossary.html) states the following

"*The rate of aging is typically greatest during the first 30 to 60 days after which time the aging rate decreases. The following factors effect crystal aging: adsorption and desorption of contamination on the surfaces of the quartz, stress relief of the mounting and bonding structures, material outgassing, and seal integrity.*"

One of the effects of over-driving the crystal out of its specified conditions may be aging of the crystal which is expected to result in frequency shift. From speaking to various crystal manufacturers, we have been informed that the majority of the shift due to aging usually occurs in the first 45–60 days or so.

In general, it is recommended that a designer always make sure that the power dissipated by the crystal is within the crystal manufacturer's specifications. Over-driving the crystal *may* have adverse effects on the crystal performance and accuracy. It is also recommended that the user refer to the crystal manufacturer's recommendations on the various effects of driving a crystal beyond its specified values.

The CY7C68013 requires a crystal with load capacitors that are between 20 pF and 33 pF, while the CY7C68013A requires a crystal with load capacitors of 12 pF. During the development phase, for test purposes, an existing BOM that has a crystal with 20 pF to 33 pF should be used to operate a CY7C68013A at room temperature.

There has been reports from few FX2LP customers that the use of the same crystal with 16-pF or 20-pF load capacitance does not seem to cause any problems. Please be informed that even though the crystal with load capacitance of 16 pF or 20 pF appears to work (and most probably will work for a long time) we are unable to provide test reports or any test data on this, as the part was designed and tested to use the crystal as specified above.

Using a 16-pF or 20-pF crystal, or for that matter any other standard load capacitance, may and most probably will work as indicated by the discussions we have had with various crystal manufacturers. But using this is at the customers discretion as the FX2LP part was only tested and designed for a 12-pF, 24-MHz crystal. Please consult with the specific crystal manufacturer for information on the various effects of driving a crystal beyond its specified values. When a crystal is used in the design using FX2LP, Cypress recommends that for proper operation the load capacitance of the crystal should be 12 pF.

Changes on AVCC/AGND Pin Functionality

As far as PCB changes are concerned, there are no major ones. Both FX2 and FX2LP run on a single 3.3V supply. There are two additional AVCC/AGND pins on the FX2LP that can be re-routed on the PCB to provide additional filtering. These two additional pins exist in the 56-, 100-, and 128-pin packages.

For the 128-pin TQFP package, AVCC is pin 17 (was VCC on the FX2), and AGND is pin 20 (was GND on the FX2). Pin 17 of the FX2LP128 pin package does not need a duplicate of the pin 10 AVCC filter network. It can be wired in parallel to pin 10.

The FX2LP can use the same filter network as the FX2 for AVCC. The FX2LP analog ground (pin 20 in 128-pin package) does not need to be isolated. It can be connected to the digital ground. Other changes made to the chip do not affect all designs.

Feature Changes

An overview of the feature changes/additions in the FX2LP (CY7C68013A) are listed below:

- Lower power
- Enabling pull-up on D+
- Disabling high speed chirp via EEPROM config byte
- Expanded internal code/data RAM
- ECC generation on GPIF data
- Zero-length in-packets with no firmware intervention and Data PID sequencing in isochronous IN transfers
- Additional Package with more GPIOs (CY7C68015A).

Lower Power

The FX2LP uses a different process then the FX2. The major result of this change is to reduce the power consumption of the chip. The lower current is obtained just by using the FX2LP with the required crystal modifications. This configuration meets all USB bus powered requirements of unconfigured current (100 mA) and suspend current (500 µA).

As a result of this lower power, to meet the unconfigured current limit, it is no longer necessary to use the double enumeration procedure where the device first enumerates in full speed with a current draw below 100 mA and then disconnects and reconnects as a high speed device as described in the application note *Bus-Powered Enumeration with the FX2*. If an existing design uses this procedure the designer MUST remove the procedure in design. For new designs using FX2LP, there is no concern as the part does meet the 100-mA limitation requirement for unconfigured current while operating in either full or high speed.

Enabling Pull-up on D+

There is a minor difference with respect to when the internal logic enables the pull up on D+ to signal an attach event to the host. In the case of the FX2, the pull-up on D+ is enabled on power-up. In the case of the FX2LP, the pull-up on D+ is enabled when the reset is released (in a deasserted state).

On plug in, the FX2 enables the pull-up on D+ signaling at attach event to the host. If the reset is held active for longer than 100 ms, an attach signal will be sent to the host and the host will begin its enumeration sequence (after 100 ms from when the attach is detected), while the FX2 is still held in reset. Section 7.1.7.3 (page 150) of the USB 2.0 specification, provides further information on the debounce interval (delta t3). While using the FX2 Cypress recommends that a reset time of 10 ms with an RC network of 100K/0.1 µF be used.

The FX2LP has a more flexible reset timing requirement. As the FX2LP enables the pull-up n the D+ once the RESET is deasserted, there really is no restriction on the reset timing as the host will only receive an attach signal when the RESET is released.l

Disabling High Speed Chirp via EEPROM Config Byte

During power-on sequence, the operating speed of the FX2 device defaults to high-speed. The FX2 device has the capability of disabling the high-speed chirp state machine using the Cypress internal register CT1. The 8051 can set or clear bit 1 of the CT1 register anytime. On re-enumeration (disconnecting and then reconnecting) the FX2 device will enumerate with the chirp state machine disabled if this bit of the CT1 register is set to 1. So on a disconnect event followed by a re-connect, the device will re-enumerate as a full-speed only device.

The chirp state machine can also be disabled on power-up, by setting bit 7 of the configuration byte of the EEPROM. During power-up sequence, the core will copy this bit setting to bit 1of the CT1 register and the device will enumerate as a full-speed device. Once enumerated as a full-speed device, the 8051 may enable the chirp state machine anytime by clearing bit 1 of the CT1 register. On re-enumeration the same device will enumerate as a high-speed device.

In the case of FX2LP, the device also defaults to the high-speed mode of operation: bit 1 of the CT1 register defaults to 0. After the device has powered-up with the chirp state machine enabled (default), it can be switched to a different mode of operation by having the 8051 change bit 1 of the CT1 register.

If no EEPROM is used, the device will operate in its default high-speed mode. If using an EEPROM, the chirp state machine status is determined by the setting of bit 7 of the configuration byte of the EEPROM. The behavior of the FX2LP chirp state machine is different than the FX2 when bit 7 of the configuration byte of the EEPROM is set to 1 (chirp state disabled on power-up).

The CT1 register and the EEPROM control bit (bit 7 of the configuration byte) behave differently in FX2LP than in FX2. In FX2, if the EEPROM control bit that forces USB full-speed operation is set, FX2 comes up in full-speed mode, and upon re-enumeration FX2 is capable of re-enumerating on the USB bus in high-speed mode (if the 8051 has cleared bit 1 of the CT1 register to enable high-speed mode). In the case of FX2LP, if the full-speed control bit of the EEPROM is set, the device will ONLY come up in full speed mode, even after USB re-enumeration.Setting or clearing this bit by the 8051 has no effect on enabling or disabling the chirp state machine when bit 7 of the configuration byte of the EEPROM is set to 1. If it is set to 0, FX2LP behaves the same as the FX2. In other words when bit 7 of configuration byte is set to 0 (chirp enabled) the FX2LP comes up in high speed mode and the 8051 may switch the mode by changing bit 1 of CT1 register anytime followed by a disconnect and reconnect event.

If the existing FX2 application is bus powered and uses the double enumeration sequence (which is a recommended workaround) to meet the unconfigured current requirements of the USB-IF compliance test, then the application will not behave the same when replaced with the FX2LP. If replacing the part with FX2LP, when the device enumerates with the high speed chirp disabled (control bit of the configuration byte of the EEPROM set), on renumeration, the device will fail to enumerate as a high speed device even though the 8051 had cleared bit 1 of the CT1 register. As stated in the *"Bus Powered Enumeration with FX2"* application note, the full speed mode trick upon initial plug was done to get the unconfigured power down to the 100-mA range. As FX2LP power

is 50–60 mA max., not meeting the unconfigured current limit when using the device as bus powered, is no longer an issue—there is no need to set this control bit in the EEPROM anymore. The workaround is not required anymore. Just have the FX2LP application enumerate in USB high-speed mode from the start.

In order for an FX2 bus powered application that uses double enumeration sequence to behave the same when replaced with FX2LP, all you need to do is set the control bit of the EEPROM to 0 (chirp enabled) and can leave the firmware 'as is' with the double enumeration workaround code in it.

Expanded Code/Data RAM

The FX2LP has 16 Kbytes of internal Code/Data RAM, where the FX2 had only 8 Kbytes. The additional RAM is located in the address space of 0x2000 to 0x3FFF. If the firmware of the existing design is completely internal to the FX2, no changes are required to use the FX2LP. If the FX2 design had RAM at this location, no changes are required. The FX2LP will access the internal RAM instead of the external RAM.

If there was either memory mapped ROM (any non-volatile memory) or memory mapped I/O within these locations, they must be mapped to new locations and the firmware should be relinked. In the limited number of designs that require this change, just a logic change to a FPGA or programmable logic array for hardware memory decoding and changing the target location of the external code within the compiler/linker is required.

In most designs it is felt that the external memory map would not have used this location in memory. Less logic is required to locate the memory at higher locations and therefore it is believed that most designs would have used a higher address, such as 0x8000, to start the external memory. If this is the case, no modifications, other then the required crystal modifications, are required.

ECC Generation on GPIF Data

This is a new feature and does not affect existing designs. If ECC generation is to be added to an existing design there are additional registers that enable this function.

The FX2LP can be configured to either calculate two separate 256-byte ECCs on two consecutive 256-byte blocks of data, or alternatively one single 512-byte ECC on a 512-byte block of data. Once the 8051 resets the ECC calculation by writing any value to ECCRESET, the FX2LP will calculate ECC on any data bytes that transfer across the GPIF or Slave FIFO interface. The FX2LP will stop ECC calculation once 512 bytes have been processed and it will wait for a new ECC reset from the 8051 before it commences any new calculations.

The additional registers for this function are:

ECCCFG:	Configuration register (256/512)
ECCRESET	Reset ECC-byte registers to zero
ECC1B0,	This is the second eight bits of the line parity on the first 256-byte block or the 512-byte block.
ECC1B1	Lower eight bits of line parity on first 256-byte block or lower eight bits of line parity on 512-byte block.
ECC1B2	This is the 6-bit column parity on first 256-byte block or 6-bit column parity on and

upper two bits of line parity for 512-byte block.

ECC2B0	This is the second eight bits of the line parity. on the second 256-byte block
ECC2B1	Lower eight bits of line parity on second 256-byte block
ECC2B2	This is the 6-bit column parity on the second 256-byte block

(For column and line parity see Smartmedia Specification.)

See Technical Reference Manual for check/correct sample code.

Zero-length in Packets with No Firmware Intervention and Data PID Sequencing for ISO Transfers

The FX2LP has the capability of sending a zero length isochronous data packet (ZLP) when the host issues an IN token to an isochronous IN endpoint FIFO and the SIE does not have any data packets available.

This feature is very useful when designing high-bandwidth isochronous applications. When an isochronous IN endpoint is configured for greater than one packet per microframe, there is a possibility of the core not having more than one packet available in a microframe. In this case, when the host issues an IN token, the FX2LP core will automatically send a zero length packet with the appropriate data PID. Hence avoiding the occurrence of a scenario where the host may encounter a turnaround time-out error on not receiving any data when requesting more than one packet per microframe.

In version 1.1 of the Technical Reference Manual, registers EPxISOINPKTS defines an additional bit called: ADDJ. This bit defaults to a zero value. In this condition, FX2LP operates the same as the FX2. This bit (AADJ) is a RESERVED bit in FX2LP and should be left to its default value of 0.

The auto adjust (AADJ) feature was useful when designing with the FX2LP engineering samples provided at the early stages of the FX2LP development. These engineering samples did not have the ability to issue a zero length isochronous packet automatically and hence were prone to running into a DATA PID mismatch scenario when dealing with high bandwidth ISO IN transfer (please refer to the *"Streaming Data Through Isochronous/Bulk Endpoints on EZ-USB FX2"* application note for further information on DATA PID mismatch issue). The auto adjust feature was a partial workaround to the data PID mismatch issue and in order to use this workaround, the wMaxPacketSize that could be defined in the isochronous endpoint descriptor was limited to 1024 bytes. The latest (production) version of the FX2LP is capable of issuing a zero length packet automatically when there is no data packet available in the core, which resolves the issue regarding the data PID mismatch. Hence the auto adjust feature is really not necessary to be used when using this production version of the FX2LP silicon. This latest version of the silicon requires that this AADJ bit be left to its default value of 0 and be treated as a reserved bit. The next version (after 1.1) of the Technical Reference Manual will update the usage of this bit to be treated as a reserved bit.

Using this ZLP improvements the part has addressed the Data PID mismatch issue and using this feature has resulted in increasing the data throughput tremendously.

Package Changes

Additional options have been made available in the packaging of the FX2LP part. Additional configurations are available in the 56-pin packages. These configurations allow for two additional GPIO pins. These parts are the part number CY7C68015A/CY7C68016A available in both a QFN and a SSOP package. As in FX2, all FX2LP parts are available in lead-free packages. The following table lists the FX2 parts and the respective FX2LP part that may be used to replace the FX2.

CY7C68014A and CY7C68016A are Ideal for battery powered applications as they have an ultra-low suspend current of 100 μA (typical). CY7C68013A and CY7C68015A which have a low suspend current of 300 μA (typical) are Ideal for non-battery powered (self or bus powered) applications.

EZ-USB FX2 Part Number	EZ-USB FX2LP Part Number	Package Description
CY7C68013-56PVC	CY7C68013A-56PVXC or CY7C68014A-56PVXC	56-pin SSOP
CY7C68013-56LFC	CY7C68013A-56LFXC or CY7C68014A-56LFXC	56-pin QFN
CY7C68013-100AC	CY7C68013A-100AXC or CY7C68014A-100AXC	100-pin TQFP
CY7C68013-128AC	CY7C68013A-128AXC or CY7C68014A-128AXC	128-pin TQFP

Development Tool

The FX2LP has a development kit similar to that of the FX2. The part number for this kit is CY3684. The development kit for the FX2LP contains a development board, cables, documentation and a development CD.

The CD has electronic copies of the Technical Reference Manual, the data sheet, schematics and gerbers for the development board, firmware examples, drivers (CyUSB.sys), the USB Developer's Studio control panel and evaluation version of the Keil's μVision2 Compiler. Items of interest that a developer will want to use as references are:

- *EZ-USB® Technical Reference Manual*
- CY7C68013A/CY7C68015A data sheet
- CYStream–Streaming Over USB with Isochronous and Bulk Transfers (P/N CY4603)
- USB Developer's μ-Studio (P/N CY4604).

Redesigning an Existing FX2 Application to an FX2LP Application

Following are the main items to consider while replacing the FX2 in an existing application with an FX2LP part:

- Make sure to replace the crystal with the appropriate load capacitors. The FX2LP requires a crystal with load capacitors of 12 pF.

- Is the existing FX2 application bus-powered and has the double enumeration workaround for meeting the unconfigured current limit of 100 mA? If so, set the control bit of the EEPROM to 0 (chirp enabled). You may opt to either leave

in or remove the double enumeration workaround in the firmware.

- Check the code location to make sure if the existing FX2 application uses memory mapped ROM (any non-volatile memory) or memory mapped I/O within the address space of 0x2000 to 0x3FFF. If so, they must be mapped to new locations and the firmware should be relinked. In the limited number of designs that require this change, just a logic change to a FPGA or programmable logic array for hardware memory decoding and changing the target location of the external code within the compiler/linker is needed. If the existing FX2 design has RAM at this location (0x2000 to 0x3FFF), no changes are required while replacing the part with FX2LP.

- Does the FX2 application use high-bandwidth Isochronous IN transfer? If so, does it have a workaround (on the host end or the device end) for handling the possible occurrence of a scenario of data PID mismatch: additional hardware, external logic, or software on the host end to handle the scenario? If so, you may consider removing the additional logic/code as the FX2LP has resolved this data PID mismatch issue. You may also choose to not remove the designed workaround for ease of drop-in replacement with FX2LP

Note that in general, when changing components such as the USB controller (FX2 to FX2LP), the USB-IF will require the certification test to be rerun. The USB controller and the board traces will have the majority of the effects on the electrical characteristics of the device and therefore the USB-IF will require the device to be retested.

Conclusion

This application note has introduced the reader to the differences between the FX2 and the FX2LP. As discussed in this application note, the only required change when using the FX2LP in place of the FX2 is the alteration of the crystal load capacitors and the load capacitance of the crystal. With exception of the load capacitance on the crystal, the crystal for the FX2LP contains the same requirements as that for the FX2. Additional features are also highlighted, but are defaulted to function as the FX2 would. This enables use of FX2LP in prior designs with minimal or none at all changes to the firmware. Due to the increased memory within the FX2LP, a limited number of designs may require a memory map change.

As with Cypress's FX2, the FX2LP is made available with world-class development tools and software support. Visit www.cypress.com for more device details and data sheet information.