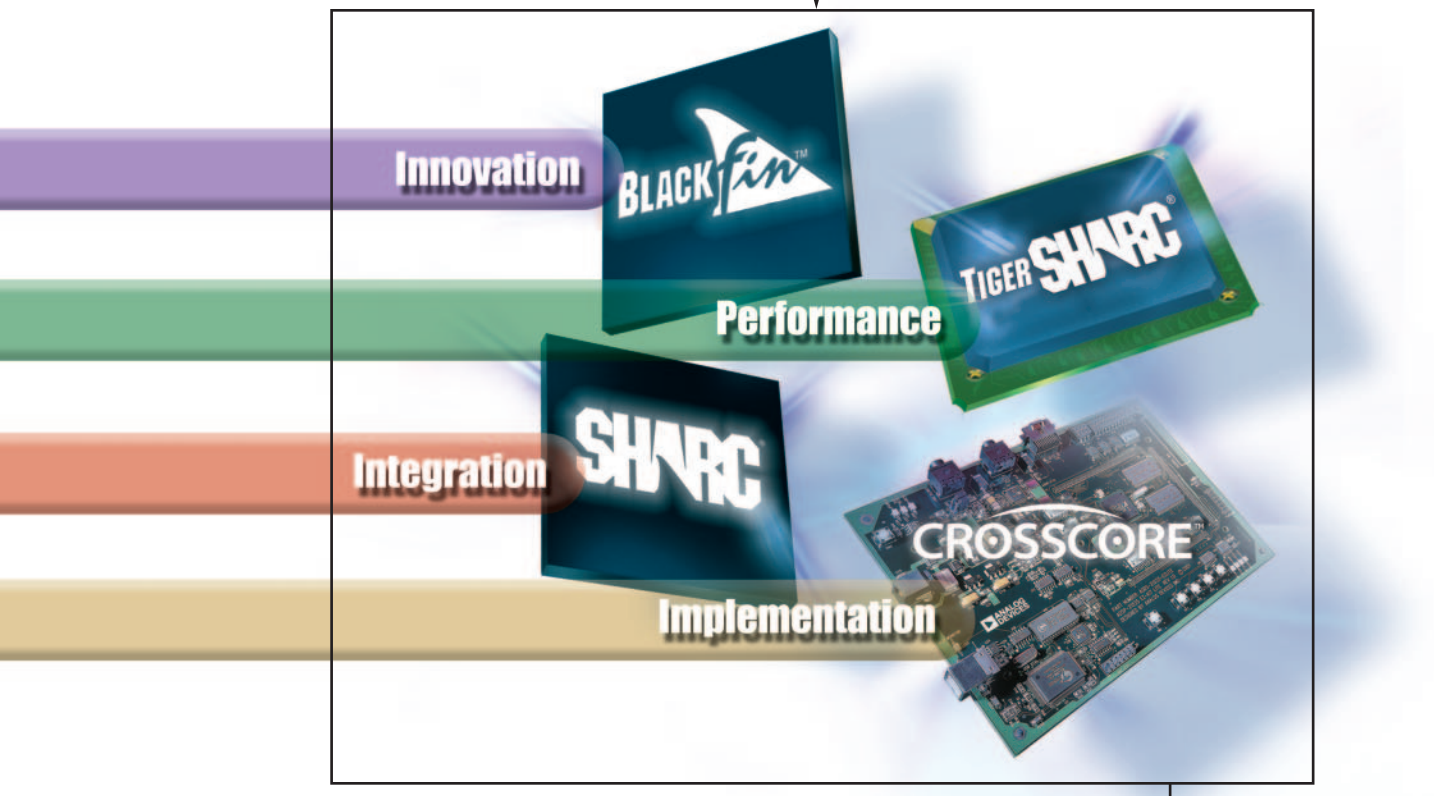
Embedded Processors and Development Tools for Digital Signal Processing Applications



2003 Edition

- Processor Selection Guides
- Development Tools
- Support Resources
- Benchmarks
- Training Workshops

ANALOG DEVICES

www.analog.com/processors

Contents

ADI Processor Portfolio

ADI's embedded architectures feature simple yet powerful programming models and are supported by high quality development tools.

Blackfin Processors
High Performance, Low Power, Processing Leadership

Based on Micro Signal Architecture (MSA), Blackfin processors enable efficient processing of video, image, audio, and voice data by combining high-performance signal processing functionality with the advantages of a RISC microcontroller instruction set. This unified programming model eliminates complexities traditionally associated with multi-processor systems consisting of individual signal and control processing elements.

Blackfin processors are ideal for:

- Portable and networked digital media appliances
- Consumer communications and network applications
- Automotive telematics and infotainment applications

TigerSHARC Processors
Highest Performance Processor for Multiprocessor Systems

ADI's TigerSHARC processors offer the best-in-class performance. They embody a breakthrough static super-scalar architecture that boasts native support of 1-, 8-, 16-, and 32-bit fixed-point and floating-point data types on a single chip. TigerSHARC processors are well-suited to signal processing applications that rely on multiple processors working together to execute computationally-intensive real-time functions.

TigerSHARC processors are ideal for:

- Wireless infrastructure such as 3G basestations and software-defined radios
- Multiprocessing applications for medical imaging, industrial, instrumentation, military markets

SHARC DSPs
Leadership in Premium Audio Applications

Using ADI's "Super" Harvard architecture, the SHARC family is optimized to enable a variety of real-time embedded signal processing applications and is known as a leader in premium audio applications. The unique memory architecture – two large on-chip, dual ported SRAM blocks coupled with the sophisticated I/O processor – enables the SHARC family to sustain high-speed computation requirements of today's applications. The SHARC family is the de facto standard in premium audio, supported by a wide range of audio processing algorithms and highly integrated audio peripherals. SHARC DSPs deliver high performance and code compatibility within more than 50 products.

SHARC DSPs are ideal for:

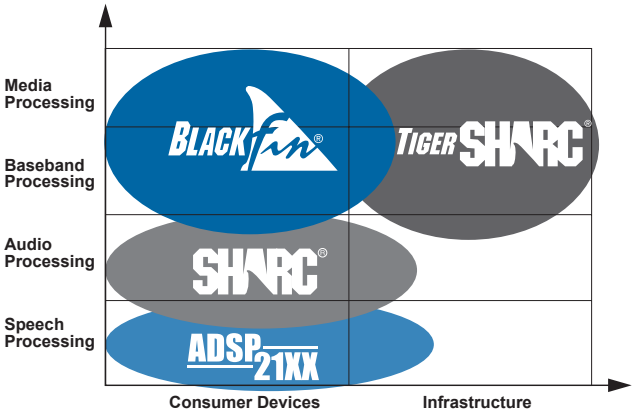
- Home theater audio systems
- Automotive audio applications
- Professional audio systems
- Industrial and instrumentation

ADSP-21xx and Mixed-Signal DSPs
Code-Compatible DSP Excellence

The ADSP-21xx family architecture is built around a common instruction set architecture. All family members are code-compatible, fixed-point 16-bit DSPs. The family offers a wide range of speed and performance options. In addition, the ADSP-2199x family of mixed-signal DSPs provides a single-chip solution with signal processing and 14-bit ADC mixed signal integration.

ADSP-21xx and ADSP-2199x DSPs are ideal for:

- Telephony
- Data acquisition
- Industrial automation
- Motor control
- Optical networking control
- Portable instrumentation



Markets and Applications

Segment	Market	Applications	Architecture
Communications	Wired Communications	Optical Networking	Blackfin, SHARC, 21xx
		Data Infrastructure	21xx
		MultiMedia over IP	Blackfin
		IP Phone	Blackfin, 21xx
		IP CPE	Blackfin, 21xx
		IP CO / Infrastructure	Blackfin, TigerSHARC
		POTS Phone	Blackfin, 21xx
		POTS CPE	Blackfin, 21xx
		POTS CO / Infrastructure	Blackfin, 21xx
		Broadband Access	Blackfin
		RAS Modem	Blackfin, 21xx
		Set-top box (as communication engine)	Blackfin, 21xx
		Video Conferencing/phone	Blackfin
		Home Networking	Blackfin, 21xx
	Wireless Comms	Basestation (2G, 2.5G, 3G)	TigerSHARC
		Access (broadband) (i.e. 802.16 ..)	Blackfin, TigerSHARC
		Handset	Blackfin, 21xx
		Satellite Phone	Blackfin, 21xx
		Portable Access Device	Blackfin, 21xx
		Cellular Location System (Network)	Blackfin, SHARC
		Cellular Digital Camera	Blackfin
Consumer	PDA	Multimedia Processing	Blackfin
	Toys	Interactive Toys	Blackfin, 21xx
		Video Game Console	Blackfin
	Computer	Printer	Blackfin
	Entertainment	TV-Audio	SHARC, Blackfin
		TV-Video	Blackfin
		Home Theater AVR	Blackfin, SHARC
		eMedia (Digital Network Media Devices)	Blackfin
		Home Server AVR / Networked	Blackfin
		DVD	Blackfin
		PVR (non networked)	Blackfin
		Portable Digital Audio (e.g., MP3 Player)	Blackfin
		Satellite Radio/Digital Radio	Blackfin
		Digital Still Camera	Blackfin
		Digital Video Camera	Blackfin
		Portable Media Player/ Portable Entertainment Console	Blackfin
		Digital Home Video Appliance	Blackfin
		Set top box (non communication features)	Blackfin
		Prosumer Audio	SHARC, Blackfin
		Professional Audio/ Broadcast	TigerSHARC, SHARC

Segment	Market	Applications	Architecture
Automotive	Car Multimedia and Telematics	Telematic	Blackfin
		Navigation	Blackfin, 21xx
		Car Audio	SHARC, Blackfin
		Car Video Processing	Blackfin
		Satellite Radio/Digital Radio	Blackfin, 21xx
		Handsfree	Blackfin, 21xx
		Microphone Array	Blackfin, 21xx
	Body Control	"x"-by-Wire	Blackfin, 21xx
		Biometrics	Blackfin, SHARC, 21xx
	Safety Systems	Smart Airbag	Blackfin, SHARC
		Adaptive Cruise Control	Blackfin,SHARC
		Collision Avoidance	Blackfin, SHARC
		ABS	Blackfin, SHARC
		Electronic Suspension Control	Blackfin, 21xx
	Engine and Powertrain Control	Engine Controls	Blackfin, SHARC, 21xx
Industrial and Instrumentation	Medical	Ultrasound	TigerSHARC
		CT	TigerSHARC
		MRI	TigerSHARC
		X-Ray	TigerSHARC
		Portable Medical	Blackfin
		Diagnostic	Blackfin, TigerSHARC
		Patient Monitoring	Blackfin, TigerSHARC
	PDS	Scanner	Blackfin, SHARC
		Slot/Vending machine	Blackfin
	Test/ Measurement Equipment	ATE	TigerSHARC, SHARC
		Communication	TigerSHARC, SHARC
		Measurement	Blackfin, TigerSHARC, SHARC
	Industrial	Verification and Biometrics	Blackfin,TigerSHARC, SHARC, 2199x
		Robotics	Blackfin,TigerSHARC, SHARC, 2199x
		Data Acquisition	Blackfin,TigerSHARC, SHARC, 2199x
		Power Control	Blackfin,TigerSHARC, SHARC, 2199x
		Industrial Control	Blackfin,TigerSHARC, SHARC, 2199x
		Metering	Blackfin,TigerSHARC, SHARC, 2199x
		Video and Surveillance Systems	Blackfin
		Vision Systems	Blackfin,TigerSHARC, SHARC, 2199x
		Motor Control	Blackfin,TigerSHARC, SHARC, 2199x
Mil/Aero	Guidance	Radar	TigerSHARC
		Sonar	TigerSHARC
	Mil	Smart Munitions	TigerSHARC
		Location	Blackfin, TigerSHARC
		Comms	Blackfin, TigerSHARC
	Aero	Entertainment	Blackfin
		Control	Blackfin

Blackfin® Processor Key Products
Recommended for New Designs

Model	Max MMACS	L1 Memory Bytes	L2 Memory Bytes	Operating Voltage Core, I/O	Pin/Pkg	Price/1K*	Status
ADSP-BF533SKBC-600	1200	148K	-	0.7-1.2V/3.3V	160-MBGA	$23.50	Samples Now Release 4Q03
ADSP-BF533SBBC-500	1000	148K	-	0.7-1.2V/3.3V	160-MBGA	$20.00	Samples Now Release 4Q03
ADSP-BF532SBBC-400	800	116K**	-	0.7-1.2V/3.3V	160-MBGA	$11.50	Samples Now Release 4Q03
ADSP-BF532SBST-300	600	116K**	-	0.7-1.2V/3.3V	176-LQFP	$11.50	Samples 3Q03 Release 1Q04
ADSP-BF531SBBC-400	800	84K**	-	0.7-1.2V/3.3V	160-MBGA	$8.00	Samples Now Release 4Q03
ADSP-BF531SBST-300	600	84K**	-	0.7-1.2V/3.3V	176-LQFP	$7.00	Samples 3Q03 Release 1Q04
ADSP-BF535PKB-350	700	52K	256K	1.0-1.6V/3.3V	260-PBGA	$44.80	Released
ADSP-BF535PBB-300	600	52K	256K	1.0-1.5V/3.3V	260-PBGA	$35.20	Released
ADSP-BF535PKB-300	600	52K	256K	1.0-1.5V/3.3V	260-PBGA	$32.00	Released
ADSP-BF535PBB-200	400	52K	256K	1.0-1.5V/3.3V	260-PBGA	$30.00	Released

Processor	Evaluation Development Platform	Emulator	VisualDSP++ Development Software
ADSP-BF531 ADSP-BF532 ADSP-BF533 ADSP-BF535	ADDS-BF533-EZLITE $295 ADDS-BF533-1-EZEXT $195 ADDS-BF535-EZLITE $295	ADDS-APEX-ICE $4000 ADDS-HPPCI-ICE $4000	VDSP-BLKFN-PC-FULL $3500 VDSP-BLKFN-PCFLOAT $4250

Note: DSP tools pricing is US dollars and subject to change at anytime. Volume discounts are available for VisualDSP++. Please contact your local ADI sales representative or distributor for more information.

Packages: LQFP = Low-profile Quad Flat Pack
MBGA = Mini Ball Grid Array
PBGA = Plastic Ball Grid Array

* US Dollars. Lowest grade suggested resale price per unit in 1000 unit quantities
All pricing is budgetary – subject to change

** Includes 32K of user-definable ROM

TigerSHARC® Processor Key Products
Recommended for New Designs

32-Bit Generic	Max MFLOPS	Max MMACS	On-Chip Memory	Operating Voltage Core, I/O	Pin/Pkg	Price*	Status
ADSP-TS101S	1800	32 bit- 600 16 bit-2400	6 Mbits	1.2V/3.3V	625-PBGA 484-PBGA	$207.00	Released

Processor	Evaluation Development Platform	Emulator		VisualDSP++ Development Software	
ADSP-TS101S	ADDS-TS101S-EZLITE $995	ADDS-APEX-ICE	$4000	VDSP-TS-PC-FULL	$3500
		ADDS-HPPCI-ICE	$4000	VDSP-TS-PCFLOAT	$4250

Note: DSP tools pricing is US dollars and subject to change at anytime. Volume discounts are available for VisualDSP++.
Please contact your local ADI sales representative or distributor for more information.

SHARC® DSP Key Products
Recommended for New Designs

32-Bit Generic	Max MFLOPS	On-Chip Memory	Operating Voltage Core, I/O	Pin/Pkg	Price*	Status
ADSP-21161N	600	1 Mbit	1.8V/3.3V	225-MBGA	$24.63	Released
ADSP-21160M	480	4 Mbits	2.5V/3.3V	400-PBGA	$145.00	Released
ADSP-21160N	600	4 Mbits	1.9V/3.3V	400-PBGA	$145.00	Samples Now Release 2Q03
ADSP-21065L	198	544 Kbits	3.3V/3.3V	208-MQFP 196-MBGA	$19.50	Released

Processor	Evaluation Development Platform	Emulator		VisualDSP++ Development Software	
ADSP-21161N	ADDS-21161N-EZLITE $495				
ADSP-21160M	ADDS-21160-EZLITE $595	ADDS-APEX-ICE	$4000	VDSP-SHARC-PC-FULL	$3500
ADSP-21160N	ADDS-21160N-EZLITE $650	ADDS-HPPCI-ICE	$4000	VDSP-SHARC-PCFLOAT	$4250
ADSP-21065L	ADDS-21065L-EZLITE $299				

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Packages: PBGA = Plastic Ball Grid Array
PQFP = Plastic Quad Flat Pack
MBGA = Mini Ball Grid Array

* US Dollars. Lowest grade suggested resale price per unit in 1000 unit quantities
All pricing is budgetary – subject to change

ADSP-21xx 16-Bit DSP Key Products
Family Overview

ADSP-21xx	Max MMACS	Program Memory Words	Data Memory Words	Operating Voltage Core, I/O	Pin/Pkg	Price*	Status
ADSP-2191M	160	32K	32K	2.5V/3.3V	144-LQFP/144-MBGA	$16.85	Released
ADSP-2195M	160	32K**	16K	2.5V/3.3V	144-LQFP/144-MBGA	$13.90	Released
ADSP-2196M	160	24K**	8K	2.5V/3.3V	144-LQFP/144-MBGA	$11.10	Released
ADSP-2188N	80	48K	56K	1.8V/3.3V	100-LQFP/144-MGBA	$26.00	Released
ADSP-2189N	80	32K	48K	1.8V/3.3V	100-LQFP/144-MGBA	$21.00	Released
ADSP-2187N	80	32K	32K	1.8V/3.3V	100-LQFP/144-MGBA	$17.00	Released
ADSP-2185N	80	16K	16K	1.8V/3.3V	100-LQFP/144-MGBA	$9.50	Released
ADSP-2186N	80	8K	8K	1.8V/3.3V	100-LQFP/144-MGBA	$7.25	Released
ADSP-2184N	80	4K	4K	1.8V/3.3V	100-LQFP/144-MGBA	$5.75	Released
ADSP-2188M	75	48K	56K	2.5V/3.3V	100-LQFP/144-MBGA	$28.00	Released
ADSP-2189M	75	32K	48K	2.5V/3.3V	100-LQFP/144-MBGA	$23.00	Released
ADSP-2185M	75	16K	16K	2.5V/3.3V	100-LQFP/144-MBGA	$10.00	Released
ADSP-2186M	75	8K	8K	2.5V/3.3V	100-LQFP/144-MBGA	$7.50	Released

Mixed Signal DSP Key Products
Family Overview

ADSP-2199x	Max MIPS	Program Memory Words	Data Memory Words	Operating Voltage Core, I/O	Pin/Pkg	ADC	Price*	Status
ADSP-21990	160	4K	4K	2.5V/3.3V	176-LQFP 196-MBGA	14-Bit 20 MSPS	$19.25	Released
ADSP-21991	160	32K	8K	2.5V/3.3V	176-LQFP 196-MBGA	14-Bit 20 MSPS	$22.55	Released
ADSP-21992 with CAN	160	32K	16K	2.5V/3.3V	176-LQFP 196-MBGA	14-Bit 20 MSPS	$24.75	Released

Processor	Evaluation Development Platform		Emulator		Development Software	
ADSP-218xM/N	ADDS-2189M-EZLITE	$495	ADDS-218X-ICE-2.5V	$1995	VDSP-21XX-PC-FULL	$3500
ADSP-219x	ADDS-2191-EZLITE	$495	ADDS-APEX-ICE	$4000	VDSP-21XX-PCFLOAT	$4250
ADSP-2199x	ADDS-21992-EZLITE	$495	ADDS-HPPCI-ICE	$4000		

Note: DSP tools pricing is US dollars and subject to change at anytime. Volume discounts are available for VisualDSP++. Please contact your local ADI sales representative or distributor for more information.

Packages: LQFP = Low-profile Quad Flat Pack
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* US Dollars. Lowest grade suggested resale price per unit in 1000 unit quantities
All pricing is budgetary – subject to change

** Includes 16K words ROM

Development Tools

Development tools from Analog Devices are one of the industry's most complete lines, from the economical EZ-KIT Lite™ evaluation kits to an integrated development environment. These tools are easy to learn and easy to use, and allow designers to bring processor-based products to market quickly and efficiently.

VisualDSP++ Integrated Development Environment

VisualDSP++™ is a comprehensive toolset that supports all ADI processor families. VisualDSP++ enables design engineers to easily develop, debug, and deploy code throughout the research, design, development, and test stages of any project. VisualDSP++ integrates all of the code generation tools below:

- Assembler
- Linker
- Simulator
- C/C++ compiler
- Debugger
- PROM splitter
- Graphical plotting
- Expert Linker
- Math, DSP and C/C++ runtime library
- Integrated develoment environment
- VisualDSP++ Kernel
- Statistical profiling
- VisualDSP++ Component Software Engineering

(ADSP-218x does not have C++ support)

EZ-KIT Lite™ Evaluation Kit

The EZ-KIT Lite provides an easy way to evaluate the power of ADI's processors and begin to develop applications. These systems consist of a stand-alone evaluation board and an evaluation suite of VisualDSP++ to facilitate architecture evaluations via a PC-hosted tool set. Restrictions: Software is limited for use with the EZ-KIT Lite and program memory is limited in size. With the EZ-KIT Lite users can:

- Evaluate ADI's processors
- Learn about DSP applications
- Simulate and debug applications
- Prototype applications

EZ-Extender Board

The EZ-Extender board is a separate assembly that plugs onto the Expansion Interface of some of the new EZ-KIT Lite evaluation systems. For example, the ADSP-BF533 EZ-Extender 1 enables the Parallel Peripheral Interface (PPI) on the ADSP-BF533 EZ-KIT Lite (which is the first to feature the Expansion Interface) to connect to Analog Devices High Speed Converter evaluation boards and an OmniVision camera evaluation board. It also provides breadboard area and the ability to access all pins on the EZ-KIT's expansion interface.

Emulators

Emulators provide non-intrusive target-based debugging of processor systems. Compact and easy to use, these in-circuit emulators perform a wide range of emulation functions including single-step and full-speed execution with predefined breakpoints, viewing and/or altering of register and memory contents. A serial port emulator is available for the ADSP-218x DSP family. JTAG emulators are available for all other processor families on both PCI and USB platforms.

Development Tools

Product Family	Evaluation Kit	Emulator	Development Software		
			PC-FULL	PC-FLOAT	PC-TEST
		ADDS-APEX-ICE (USB-Based) ADDS-HPPCI-ICE (PCI-Based) ADDS-218x-ICE-2.5V	VisualDSP++ IDE, Debugger, Compiler, Assembler, Linker with Emulation and Simulation Support	VisualDSP++ Floating License for NT Server	VisualDSP++ Test Drive 90-Day Free Trial
Blackfin Processors					
ADSP-BF531/2/3 ADSP-BF535	ADDS-BF533-EZLITE ADDS-BF533-1-EZEXT ADDS-BF535-EZLITE	ADDS-APEX-ICE ADDS-HPPCI-ICE	VDSP-BLKFN-PC-FULL	VDSP-BLKFN-PCFLOAT	VDSP-BLKFN-PC-TEST
TigerSHARC Processors					
ADSP-TS101S	ADDS-TS101S-EZLITE	ADDS-APEX-ICE ADDS-HPPCI-ICE	VDSP-TS-PC-FULL	VDSP-TS-PCFLOAT	VDSP-TS-PC-TEST
SHARC DSPs					
ADSP-2106x Family ADSP-21065L ADSP-21160M/N ADSP-21161N	ADDS-21061-EZLITE ADDS-21065L-EZLITE ADDS-21160-EZLITE ADDS-21161N-EZLITE	ADDS-APEX-ICE ADDS-HPPCI-ICE	VDSP-SHARC-PC-FULL	VDSP-SHARC-PCFLOAT	VDSP-SHARC-PC-TEST
21xx 16-Bit DSPs					
ADSP-2181 ADSP-218x Family	ADDS-2181-EZLITE ADDS-2189M-EZLITE	ADDS-218x-ICE-2.5V	VDSP-21XX-PC-FULL	VDSP-21XX-PCFLOAT	VDSP-21XX-PC-TEST
ADSP-219x	ADDS-2191-EZLITE	ADDS-APEX-ICE ADDS-HPPCI-ICE			
Mixed Signal DSPs					
ADSP-2199x Family	ADDS-21992-EZLITE	ADDS-APEX-ICE ADDS-HPPCI-ICE	VDSP-21XX-PC-FULL	VDSP-21XX-PCFLOAT	VDSP-21XX-PC-TEST

See pages 2-4 for development tools pricing

VisualDSP++™
Integrated Development Environment

Features

Integrated Development and Debugger Environment

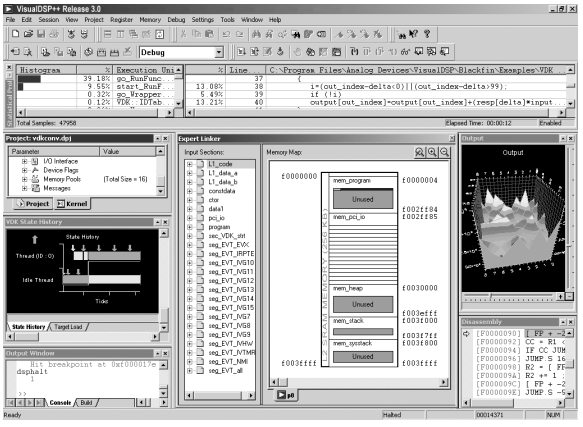
- Develop within a single interface (IDE/debugger)
- Profile and trace instruction execution of C/C++ and assembly programs
- Set watchpoints (conditional breakpoints) on processor registers and stacks, as well as program and data memory including:
  - Statistical profiling
  - MP (multiple processor support)
  - Graphical plotting
- Define all project and tool configurations through property page dialog boxes
- Set project-wide or individual file settings for debug or release mode project builds
- Create source files using an integrated, full-featured editor with syntax highlighting, advanced search/find/replace, and bookmarks
- VisualDSP++ Kernel (VDK)
- VisualDSP++ Component Software Engineering (VCSE)
- Pipeline viewer
- Cache visualization

Code Generation Key Features

- Develop applications using an optimizing C/C++ compiler
- Intersperse inline assembly statements within C/C++ source code
- Create executables using a linker that supports multiprocessing, shared memory, and code overlays
- Access numerous math, DSP, and C/C++ runtime library routines
- Expert linker
- Enhanced assembler

Overview

VisualDSP++™ is an easy-to-use project management environment, comprised of an integrated development environment (IDE) and debugger. VisualDSP++ enables management of projects from start to finish from within a single interface. The project development and debug environments are integrated, allowing movement easily between editing, building, and debugging activities.



VisualDSP++ interface

Platform and Processor Support

VisualDSP++ supports the Blackfin® Processor, TigerSHARC® Processor, SHARC® DSP, the ADSP-218x, ADSP-2199x, and ADSP-219x DSP families on Windows® 98, Windows NT, Windows 2000, and Windows XP. Refer to ADI's web site for specifications and availability at www.analog.com.

Flexible Project Management

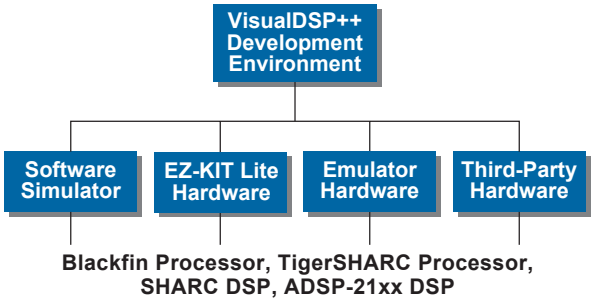
The IDE provides flexible project management for the development of applications. The IDE includes access to all the activities necessary to create and debug projects. The IDE editor allows the creation or modification of source files or viewing of listing or map files. This powerful editor is part of the IDE and includes multiple language syntax highlighting, advanced search/find/replace, bookmarks, and standard editing operations such as undo/redo, find/replace, copy/paste/cut, and go to.

VisualDSP++

The IDE allows access to the C/C++ compiler, C/C++ runtime library, assembler, linker, loader, and splitter. Specification of options for these tools is made possible through the property page dialogs. Property page dialogs are easy to use and simplify configuring, changing, and managing projects. These options may be defined once and then modified to meet changing development needs. The code generation tools can be accessed from the operating system command line.

Greatly Reduced Debugging Time

The VisualDSP++ debugger has an easy-to-use, common interface to all DSP simulators and emulators available through Analog Devices, Inc. (ADI) and from many third party partners. The debugger has many features that greatly reduce debugging time. C/C++ source can be viewed interspersed with the resulting assembly



VisualDSP++ simplifies development via common development environment across all ADI hardware and processors

code. Users can profile execution of a range of instructions in a program; set watch points on hardware and software registers, program and data memory; and trace instruction execution and memory accesses. These features enable users to correct coding errors, identify bottlenecks, and examine signal processor performance. The custom register option allows developers to select any combination of registers to view in a single window. The debugger, when used with the simulator, can also generate inputs, outputs, and interrupts to simulate real world application conditions.

With C++, developers can realize a significant increase in time to market with the ability to efficiently work with complex signal processing data types and take advantage of specialized operations without having to understand the underlying DSP architecture.VisualDSP++ simplifies development via common development environment across all Analog Devices hardware and signal processors.

VisualDSP++ Kernel

The VisualDSP++ Kernel (VDK) provides state-of-the-art scheduling and resource allocation techniques tailored specifically to address the memory and timing constraints of DSP programming. These techniques enable engineers to use example code more efficiently, eliminating the need to start from the very beginning. VDK has standard libraries and frameworks with defined APIs that allow easy inclusion of boilerplate, class libraries and value-added IP code.

Automation API

The new Automation API enables additional features and functionality to be added into the VisualDSP++ environment via an ActiveX plug-in. Third Parties will be able to seamlessly port their software to the VisualDSP++ front-end. Developers will be able to merge tool suites together to improve design, analysis and verification and will only need to learn one interface to use ADI Third Party Tools.

MP Support

VisualDSP++ multiple processor support (MP) provides a seamless interface to multiple processors on the same physical hardware. Users are able to issue parallel step, run, and halt commands to all of the applicable processors. The developer can pick and choose individual processor register or memory sets of interest by pinning those that should be updated between runs, halts and steps. This feature also eliminates screen clutter in multiple processor debugging.

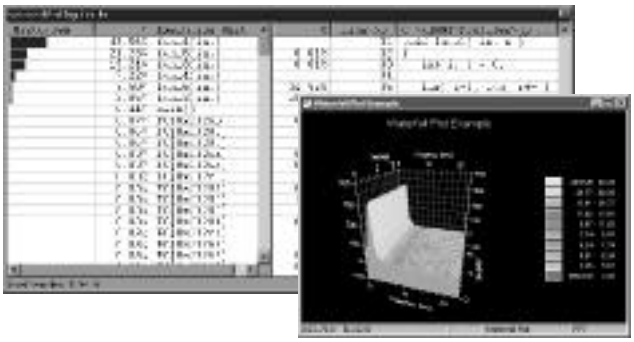
VisualDSP++'s multiprocessor dialog box and toolbar

Statistical Profiling

Statistical profiling allows for a more generalized form of profiling that JTAG emulator debug targets can take advantage of. The debugger has the ability to unobtrusively randomly sample the target processors PC and then present the user with a graphical display of the resultant samples. This allows the user to easily see where their application is spending most of its time.

Graphical Profiling

There are numerous types of plotting options, including Line, Constellation, Eye Diagrams, and 3D waterfall plots. The Plotting engine is also capable of doing some simple data processing on the data before it is displayed.



Statistical profiling and graphical window

VisualDSP++ Component Software Engineering (VCSE)

VCSE supports an Interface Definition Language (IDL) and compiler that allows developers to create and use components without having to become familiar with the detail of the model and the mechanisms it involves, allowing them to concentrate on the application itself. Component Software is designed to function as a re-usable part of a larger program. Components can easily be integrated into an application and are reusable. Integration with VisualDSP++ simplifies the process of incorporating and utilizing components from a variety of developers.

Cache

The Blackfin Processor simulator collects cache statistics that are associated with both the PC/Source Line and the Cache Line/Set. Collectable statistics are; Total Cache Accesses, Cache Hits, and Cache Misses. There will be three types of displays: Histogram by PC/Source Line, Cache Line Display where hit/miss data is associated by Cache Line/Set(way), and Summary Display of totals for hits/misses by cache.

Pipeline Viewer

The Pipeline Viewer is an ActiveX plug-in that allows a user to visually display the instruction flow through the sequencer's pipeline. Stalls, aborts and other pipeline events are graphically displayed. Visualization of the pipeline and of the pipeline events allows a user to better understand where and why latencies and stalls are being introduced into an executable. Armed with this knowledge the user can optimize an executable's instruction sequence to minimize the number of pipeline events.

Code Generation Tools

Code generation tools allow development of applications that take full advantage of the processor's architecture, including multiprocessing, shared memory, and memory overlays. Code generation tools include VisualDSP++ Component Software Engineering, C/C++ compiler, C/C++ runtime library, DSP and math libraries, assembler, linker, loader and splitter. Code generation tools work seamlessly within the VisualDSP++ environment.

VisualDSP++

C/C++ Compiler and Assembler

The C/C++ compiler generates efficient code that is optimized for both code density and execution time. The C/C++ compiler can be easily interfaced with assembly code modules. Thus, users can program in C/C++ and still use assembly for time-critical loops. The math, DSP, and C/C++ runtime library routines help shorten time to market. The Blackfin Processor, TigerSHARC Processor, SHARC DSP, ADSP-218x (ADSP-218x does not support C++) and ADSP-219x DSP family assembly language is based on an algebraic syntax that is easy to learn, program, and debug. The enhanced assembler helps the programmer write optimal assembly code by analyzing code sequences and providing feedback to the user on latencies and stalls. Feedback is given as warnings and informational messages out of the assembler and in the assembler listing.

Profile Guided Optimization

Profile Guided Optimization, or PGO, is an iterative compilation approach which uses information from previous compilations to improve the optimizer's decisions on the code being compiled. Traditionally, a compiler only compiles each function once, and attempts to generate code which will perform well in most cases by making reasonable default assumptions in the behavior of that code. With PGO, the compiler makes these decisions based on data collected during previous executions of the generated code and subsequently makes decisions about the relative importance of parts of the application rather than using the default behavior. This technique can enable large gains to be realized in the run-time performance and code density of the program.

Compiled Simulation

Traditionally, a standard simulator fetches, decodes and then simulates each instruction that an application executes. Decoding each instruction can have a significant cost, as it has to be effected each time the instruction is executed. With Compiled Simulation, the simulation compiler examines the whole application once and generates C code for each instruction in the application, essentially building a C program that is particularized to execute that one application. After the generated code has been compiled and linked with the necessary support libraries, the generated application can be used to simulate that one application very efficiently (at speed of 100 to 1000 times faster than the ordinary simulator). When running under the VisualDSP++ environment the generated compiled simulation application can be debugged in the same way as with the ordinary simulator, or be run as a stand-alone win32 executable.

Linker & Loader

The linker provides flexible system definition through linker description files (.ldf). In a single .ldf file, users are able to define different types of executables for a single or multiprocessor system. The linker resolves symbols over multiple executables, maximizes memory use, and allows common code to be shared among multiple processors. The loader supports creation of host, link port, and PROM boot images. Along with the linker, the loader allows multiprocessor system configuration with smaller code and faster boot time.

Expert Linker

The “Expert” Linker creates a graphical utility that makes it easier for users to produce Linker Description File (LDF) without having to learn the LDF syntax. The graphical representation of the commands in an LDF file also allows the engineer to manipulate the graphical representation for changes to the LDF or generation of an LDF file. The Expert Linker also allows users to optimize their placement of code.

The DSP Collaborative™
ADI's Third Party Partner Network

Tap Into the Experience and Global Reach of the DSP Collaborative

Working together to extend your design team

The DSP Collaborative partners (Analog Devices' Third Party Network) offer tools, services and solutions for a wide range of applications/markets:

- Communications
- Audio
- Medical imaging
- Speech processing
- Motor control
- Industrial automation
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When you select Analog Devices as your DSP vendor, you're broadening your design team to include the industry-leading resources of the DSP Collaborative. The DSP Collaborative is comprised of nearly 200 partners who offer more than 700 commercial products, in addition to hundreds of custom solutions that build on more than 35 years of signal processing experience found in every one of our DSPs. These partners offer consulting services as well as a wide range of commercial off-the-shelf (COTS) products. Their development tools are specifically designed to work with Analog Devices' DSP-based systems.

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- Development and evaluation boards
- COTS hardware boards
- DSP systems
- Emulators
- Debuggers

Design with Analog Devices' DSP Collaborative team approach with a proven strategy for maximizing your resources!

The DSP Collaborative™
Key Partners

Accelerated Technology

Accelerated Technology, the Embedded Systems Division of Mentor Graphics, is located in Mobile, Alabama with sales offices and distributors worldwide. By providing embedded systems developers with a focus on service, well-documented source code and industry leading non-royalty based Real-Time Operating Systems (RTOS) software, AT's RTOS software shortens time-to-market and provides a complete solution for engineers.

Accelerated Technology provides the Nucleus Real-Time Operating System for the Blackfin Processor. The Nucleus PLUS kernel provides efficient, high performance task management, inter-task communication, inter-task synchronization, memory management, and component query features. AT also provides Nucleus uiPlus and Nucleus FILE for Blackfin Processor.

http://www.acceleratedtechnology.com

Accelerated Technology®
Embedded Systems Division of
Mentor Graphics

bEST, Inc.

bEST, Inc. designs, maintains and teaches technical workshops based on Analog Devices DSP architectures as ADI's independent value added partner on a world-wide basis. Qualified full time instructors, well versed in the DSP and supporting software, teach the workshop. The workshops provide a full understanding of the fundamental architecture, I/O, low and high level programming, as well as a complete overview and support of the development tools suites. bEST provides both regularly scheduled classes in North America and Europe and in other countries based on demand. bEST also provides custom-tailored onsite classes at the customer premise on demand. In short, bEST helps Analog Devices' customers develop DSP based solutions that are bEST. In Class.

http://www.bbd.ca/best/analog

bEST
Education
Seminars
Training

BittWare, Inc.

BittWare, Inc. is a leading supplier of SHARC-based hardware and software solutions, providing its clients with innovative off-the-shelf and application-specific solutions for their high-performance, real-time signal processing and I/O requirements. Based exclusively on Analog Devices' TigerSHARC and SHARC technology, BittWare's product family includes innovative standard DSP boards and I/O peripherals on a variety of embedded platforms including PCI bus, VME, CompactPCI, PC/104, PC/104-Plus, PMC, PMC+, and standalone. From prototype to high-volume production, off-the-shelf products to application-specific solutions, BittWare is the embedded SHARC DSP solutions provider.

http://www.bittware.com

BittWare

Delphi Communication Systems

TigerSHARC Wireless Software Solutions

Tired of trying to sew together production quality software solutions from benchmark-quality algorithm libraries?

Delphi Communication Systems is a world leader in embedded software and hardware designs for wireless applications including high performance physical layer algorithms for 2.5 and 3G protocols. Delphi's wireless DSP software supports GSM/GPRS/EDGE, UMTS and CDMA2000. Delphi also offers H/W development boards, design services, protocol integration and optimization solutions for customers worldwide. Delphi's comprehensive library of wireless physical layer software, ETSI, TIA, ITU voice and video coders and Soft Frameworks are in use by customers throughout the world.

http://www.delcomsys.com

DELPHI
Communication Systems, Inc.

Epigon Audiocare Pvt. Ltd.

Epigon Audiocare Pvt Ltd brings rich experience to the Design and Development of embedded systems. Epigon Audiocare products focus on speech and digital audio technologies.

Internet Audio/Radio Chip-set: The chip-set is based on the ADSP-21161N and includes S/PDIF input and output, Ethernet connection, on board RISC processor with uClinux 2.0.38, twin ADSP-21161N processors for MPEG-4 encoding and decoding.

Audio/Speech Codec: Epigon provides the very best implementation of MP3 decoder, Layer 2 decoder, AAC-LC decoder, MP3Pro decoder and MPEG4 CELP codec on the Blackfin Processor. It also provides a specially designed proprietary wide band speech codec for VoIP applications.

http://www.epigonaudio.com

EZ-DSP

EZ-DSP, producers of TS-Lib the first and most extensive Optimized Signal and Image Processing Library for the TigerSHARC Processor, were founded to commercialize internationally recognized research into Parallel Digital Signal Processing, Knowledge Based Systems and High Performance computing. Based in Belfast, Northern Ireland, we have attracted a highly skilled team from leading academic and industrial institutions. By designing software systems which seek to increase performance, decrease costs and reduce time-to-market, EZ-DSP is focused on providing customers with a demonstrable return on investment. EZ-DSP is a center of excellence for programming the TigerSHARC Processor. We offer a wide range of services including research, design and prototyping through to product manufacture.

http://www.ez-dsp.com

Hyperception

Hyperception, Inc. was founded in 1984 to provide Digital Signal Processing (DSP) development software tools that combined the power and cost-effectiveness of two emerging technologies: the IBM PC and programmable DSPs. Hyperception supplies cost-effective products that reduce or eliminate design barriers for DSP developers.

Hyperception's software tools provide advanced technology for component-based DSP algorithm design, and speed project development. Hypersignal RIDE DSP software provides real-time design support for Analog Devices SHARC DSPs, Blackfin Processors, and provides seamless integration with the CROSSCORE tools. RIDE directly supports DSP hardware and serves as a rapid-production tool to simplify DSP design and development.

http://www.hyperception.com

KADAK Products Ltd.

Since 1978, KADAK Products Ltd. has been providing software developers with the very best real-time software foundation for their embedded systems products. Renowned for the exceptional quality of our products and documentation, we serve the most demanding of customers in aerospace, communications, process control, data acquisition, medical instrumentation, portable devices, robotics and military applications. And KADAK's no-nonsense approach to pricing and licensing means that you can COUNT ON KADAK.

KADAK Products Ltd. provides the AMX RTOS, KwikNet TCP/IP Stack and Web Server, KwikLook Fault Finder and KwikPeg GUI with graphics library. KwikNet is a TCP/IP Stack and Web Server for the Blackfin Processor.

http://www.kadak.com

The DSP Collaborative™
Key Partners

Momentum Data Systems, Inc.

MDS, with over 15 years as a DSP hardware and software supplier, is a leading supplier of Blackfin Processor hardware. Our standalone and plug in DSP boards are supported by a wide range of software allowing for reduced development time and cost. The ADSP-BF535 based Eagle-35 platform's 4 PCI slots allows creation of a custom development platform from standard PCI cards. The new ADSP-BF532 development system supports both consumer and industrial imaging development. MDS' design services group specializes in custom Blackfin Processor hardware design. MDS also offers filter and DSP system software development tools.

http://www.mds.com

MOMENTUM DATA SYSTEMS

SDL

SDL's DSP*developer* seamlessly integrates MATLAB/Simulink with Visual DSP++, dramatically slashing software development time. Applications for SHARC DSP, Blackfin, and TigerSHARC processors are rapidly prototyped and tested in the Simulink graphical, flow-chart based environment. DSP*developer* then automatically compiles, downloads, and runs the algorithms on your ADI DSP hardware in real-time. DSP*developer* supports the ADI EZ-KIT Lite and custom DSP hardware using a standard JTAG interface. Parameters can be tuned and application data viewed in real-time utilizing ADI's high-speed background telemetry capability. DSP*developer* also supports VCSE technology allowing software components created from Simulink models to be easily optimized, incorporated in a larger software project, or handed off to other developers.

http://www.sdltd.com/ADI

SDL
Embedding Intelligence

SigNumerix

SigNumerix is a leading provider of DSP software optimized for Analog Devices' DSP architectures. We deliver DSP expertise to technology leaders worldwide through our software products and engineering services.

SigNumerix specializes in developing custom software solutions for unique DSP applications. We supply comprehensive software engineering services spanning project inception through deployment. Whether your project is in the analysis, design, implementation or verification phases, we can provide the DSP expertise you require.

SigNumerix also offers a catalogue of algorithm software components addressing common DSP requirements in telephony, signal compression, and soft radio applications. These products feature excellent performance and compliance with applicable standards.

http://www.signumerix.com

SigNumerix

Transtech DSP

Transtech DSP is a total solutions pioneer and provider of high performance DSP equipment, from boards to systems. Transtech's systems use a number of processor families, including the TigerSHARC Processor and SHARC DSPs on a choice of industry standard COTS formats (VME, PCI, PMC and CompactPCI). The company's extensive product line also includes I/O boards, software tools, libraries, drivers, and enclosures to provide our customers with complete systems or custom designs. Transtech products are used to solve the most computer intensive of signal processing problems, which include radar, sonar, software radio, surveillance and medical imaging.

http://www.transtech-dsp.com

TRANSTECH™ DSP

Speech/Telephony Software Algorithms

Analog Devices' software product range consists of a broad portfolio of algorithms including speech and image/video compression, echo cancellation, fax and data modem-pumps, error correction and numerous other telephony code modules for the ADSP-21xx family of DSPs and Blackfin Processors. Typical product application areas are listed below. Our software experts provide excellent customer support, product documentation and APIs that allow rapid integration of the code into customer's new product designs.

Audio/Speech Software Algorithms
G.723.1 (5.3/6.3 kbit/s)
G.723.1A (5.3/6.3 kbit/s)
G.729 (8 kbit/s)
G.729A (8 kbit/s)
G.729B (8 kbit/s)
G.729AB (8 kbit/s)
G.728 (16 kbit/s)
G.726 (40/32/24/16 kbit/s)
G.727 (40/32/24/16 kbit/s)
G.722 (64/56/48 kbit/s)
G.711 (64 kbit/s)
Variable Rate Coders
H.32x Audio Modules
Voice Activity Detectors (VAD)
Voice AGC (Variable response time)
Comfort Noise Generator (CNG)
End to End Synchronization

Echo Cancellation Software Algorithms
G.168 Line Echo Canceller (LEC)
G.165 Line Echo Cancellation (LEC)
Acoustic Echo Cancellation (AEC – variable span)
Acoustic Echo Suppression (AES)

Data and Facsimile Modem Software Algorithms	
V.33 (14,400 bps)	V.27ter (4,800 bps)
V.32bis (14,400 bps)	V.22 (1,200 bps)
V.17 (14,400 bps)	V.23 (1,200/75 bps)
V.32 (9,600 bps)	Bell 212A (1,200 bps)
V.29 (9,600 bps)	Bell 103 (300 bps)
V.22bis (2,400 bps)	V.21 (300 bps)

Forward Error Correction (FEC) Software Algorithms	
Viterbi / Trellis	Interleavers
Reed Solomon	

Telephony Software Algorithms
Internet Audio
DTMF Detector (high performance & Bellcore, EIA, ETSI, Telstra compliant)
DTMF Encoder (high performance & ITU, Bellcore, EIA, ETSI, Telstra compliant)
Call Progress
Caller ID
RTP/JIB (Jitter Buffer)
Ring Detector
E & M Signalling
Tone Detection System (TDS)

Product Application Areas	
Internet Telephony	Security/surveillance cameras
VoN	H.324
VoIP	H.323
VoDSL	H.320
VoATM	Audioconferencing
VoCable	Videophones/Feature-phones
FoN	Digital Voice Storage
FoIP	Frame Relay
3G-Basestations	PBX Equipment
Wireless/Mobile	RAS
Gateways	DSVD
CPE/IADs/SOHO/CO	DCME
IP Phones	ISDN
Digital still cameras	Rural Radio Networks
Digital camcorders	Satellite/Microwave Systems

Speech/Telephony Software Algorithms

	Description	Peak MIPS	Average MIPS	PM (Words)	DM (Words)	PM+ (Words)	DM+ (Words)
Vocoders							
G.723.1	5.3 kbit/s	18.4	16.9	9558	11679	0	951
G.723.1	6.3 kbit/s	18.9	17.6	9558	11679	0	951
G.723.1A	5.3 kbit/s + VAD/CNG	18.6	17	9558	11679	0	951
G.723.1A	6.3 kbit/s + VAD/CNG	19.1	17.6	9558	11679	0	951
G.729	8 kbit/s	19.9	18.9	8844	4634	0	1432
G.729A	8 kbit/s (low MIPS)	10.8	10.4	7932	4677	0	1532
G.729B	8 kbit/s + VAD/CNG	20.1	19.3	12064	5405	0	1603
G.729AB	8 kbit/s (low MIPS + VAD/CNG)	12.7	10.8	11900	7700	0	1821
G.728	16 kbit/s	29	27	7947	2272	930	1743
G.726	40/32/24/16 kbit/s	8.5	8	1466	240	47	100
G.727	40/32/24/16 kbit/s	9.9	N/A	1262	252	♦	♦
G.722	64/56/48 kbit/s	12.9	N/A	1458	217	♦	♦
G.711	64 kbit/s	0.4	0.4	111	6	0	0
G.711 (II)	64 kbit/s + adaptive CNG	1	N/A	2011	1700	0	50
Echo Cancellation							
G.165/G.168	16 msec, ECD On	6.6/7.03	N/A	1100/1211	354/412	276	340
G.165/G.168	16 msec, ECD Off	4.5/4.97	N/A	1100/1211	354/412	276	340
G.165/G.168	32 msec, ECD On	9.2/10.6	N/A	1100/1211	354/412	276	340
G.165/G.168	32 msec, ECD Off	7.1/8.57	N/A	1100/1211	354/412	276	340
G.168	64 msec	15	N/A	1000	124	0	1700
G.168	128 msec (sparse)	●	N/A	●	●	●	●
AEC 64 msec span	Acoustic Echo Canceller	5.2	N/A	3153	3059	♦	♦
AEC 128 msec span	Acoustic Echo Canceller	7.2	N/A	3153	3059	♦	♦
AEC 256 msec span	Acoustic Echo Canceller	11.2	N/A	3153	3059	♦	♦
AEC 384 msec span	Acoustic Echo Canceller	15.2	N/A	3153	3059	♦	♦
Telephony							
DTMF	Encoder	0.5	N/A	68	78	2	0
DTMF	Decoder	1	N/A	1300	320	0	256
Caller ID	*Bellcore (I & II)	1.8	N/A	939	53	0	180
Call Progress	*Tone Generation	0.5	N/A	70	80	4	2
TDS	*Tone Detection System	2.5	N/A	1207	641	●	●
VAD	Voice Activity Detection	0.2-2.0	N/A	515	166	0	123
CNG	Comfort Noise Generation	1	N/A	2011	1700	0	50

This table presents only a selection of the most popular ADSP-218x, ADSP-219x and ADSP-BF53x based code modules. Above figures based on ADSP-218x. Please contact ADI or refer to the web site (www.analog.com/ada) for a full list of available algorithms.

♦ Not currently multiple instance ● Contact ADI for figures *Other Standards on request

Speech/Telephony Software Algorithms

Code Modules

The tables on the previous pages summarize the key resources used by ADI's most commonly used DSP software code modules. Please contact ADI or refer to the web site (www.analog.com/ada) for a full set of available algorithms. Apart from the addition of new modules, ADI also continuously revises existing implementations in order to further reduce MIPS and memory figures, and target latest DSP platforms using the latest tools revision.

Optimized Assembler Code

The algorithms presented have been implemented for execution on the Analog Devices ADSP-218x, and ADSP-219x series of fixed-point DSPs and are currently being ported to the new Blackfin ADSP-BF53x processor family. The code has been written in highly optimized assembler code and is hand-crafted by experienced engineers in order to provide the lowest possible use of resources (MIPS, Program Memory and Data Memory).

MIPS & Multiple Channels

It should be noted that ADI provides both peak and average MIPS figures, as any MIPS budget should use peak figures in order to choose a processor of sufficient resources. Most of ADI's code modules have been written to be multiple-instance capable. This means multiple channels of the same function can be run on one processor. For example, 13 channels of G.723.1A can be executed concurrently on a 300 MHz Blackfin ADSP-BF53x Processor.

Program & Data Memory

Running multiple channels of the same algorithm on the same processor requires only one copy of the program, thus keeping Program Memory (PM) usage low. Each additional instance of the same algorithm also requires less Data Memory (DM), due to re-use of common tables and variables. This is referred to as DM+ in the table overleaf. A similar concept applies to storage of data in Program Memory for additional instances, and is referred to as PM+ in the table.

Multiple Functions

Low MIPS and memory not only allows multiple channels of the same module to be run on one processor, it also allows many different functions/modules to be run on one processor. For example, you could run G.723.1, G.729A, G.726, G.168 and DTMF detection simultaneously on a single DSP.

Choice of Processors

The tables on the previous pages allow you to calculate how many MIPS and how much memory will be required by a given set of functions. Knowing these figures, and allowing for any user-specific shell or functions, will enable you to select the most appropriate processor (of sufficient resources) from the ADSP-218x, ADSP-219x, and Blackfin ADSP-BF53x product range. With the release of the new 600 MHz based ADSP-BF53x core comes an even higher channel density capability per processor. Added benefits of the higher MIPS processors include lower power consumption per channel and lower board space per channel.

Standards Compliance & Code Quality

ADI code modules are compliant with international standards such as the International Telecommunications Union (ITU) and the voice coders are 100% bit compliant with the ITU test vectors. ADI's algorithms have been extensively tested, are used by numerous companies world-wide and have proven interoperability. Our code modules have a common Application Programming Interface (API) based on a memory mapped interface scheme. Detailed specification sheets are available for download from the ADI web site (www.analog.com/ada). Other support documentation includes developer's guides and test reports.

Commercial Aspects

ADI can provide demonstration code for evaluation purposes and has excellent customer support to assist with selection and integration issues. Specialized customization and consulting services are also available. ADI provides flexible pricing and licensing arrangements. The benefits of licensing ADI's code, compared to in-house development, include improved time-to-market, experienced support, reduced risk, controlled cost and the ability to allocate resources to other projects.

To Order

Web: www.analog.com/ada
Email: ada.info@analog.com

Benchmarks
Comparing DSPs

To truly assess a processor's performance, you have to look beyond MHz, MIPS, or MFLOPS. There are many attributes which may be more accurate predictors of real-time signal processing performance.

Circular Buffers

Circular buffers allow a region of memory to be continually accessed without explicit program interaction. The buffer uses a pointer that automatically resets to the beginning of the buffer (wrap around) if the pointer is advanced beyond the last location in the buffer. Circular buffers are a key feature of DSP routines. Multiple buffers are used in the same routine to store filter coefficients and implement a delay line of input samples. Performance suffers if the DSP core has to perform pointer calculations along with the calculations for the routine. Performance also suffers if the DSP core only supports one circular buffer and must save and restore address registers to implement multiple buffers.

ADI's processors have hardware support for multiple circular buffers, eliminating processor overhead for address calculations.

Data Registers

The number of general-purpose data registers available can impact the code performance. Fewer registers require intermediate results to be stored in memory decreasing performance and increasing the load on the memory bus.

ADI products feature a secondary register set which allows for quick context saves when interrupts occur, rather than delaying responses to the interrupt while all register values are saved to memory.

DMA Channels/Non-Intrusive DMA

The DMA (Direct Memory Access) channels transfer data between an external source and the DSP's on-chip memory. With DMA channels, data transfers occur without the core processor having to execute data movement instructions. For example, the overhead clock cycles used to move data for an FFT can add a significant amount of time to overall algorithm execution. With multiple DMA channels available, all data transfers happen without core involvement, eliminating any overhead clock cycles.

One of the strengths of Analog Devices' processor architecture is that these DMAs do not interfere with the core operation. This capability is referred to as non-intrusive or zero-overhead DMA.

Interrupt Latency

Interrupt latency is a measure of how quickly a processor responds to an interrupt. Quick response is important especially in real-time processing. For example, an interrupt might indicate the availability of data which is only available for a finite amount of time. Therefore, fast response is critical or the data will be lost.

ADI products feature fast interrupt response time for quick execution of interrupt service routines.

Multiprocessing Support

Even with the powerful DSPs available today, there are times when the DSP task for a given system does not fit into a single DSP. Examples of such applications include sonar, radar, medical imaging, audio mixers, etc. In these cases, the ability to connect multiple DSPs in a system without any glue logic greatly simplifies the implementation.

ADI offers SHARC DSPs with specialized hardware for glueless multiprocessing.

On-Chip Memory/On-Chip SRAM Size

The amount of on-chip memory available can greatly impact system performance, cost, size, power consumption and complexity. Any time the DSP core accesses external memory, the performance can suffer. Off-chip memory often requires the core to wait additional cycles. In contrast, the DSP core can access on-chip memory at the same rate as its instruction rate. The addition of external memory adds extra components to the system which increases cost, power consumption, and complexity.

ADI leads the industry in DSP SRAM integration. ADI processors have on-chip memories which often eliminate the need for external memory in a system. Furthermore, the memory is configurable for data word size, code word size and storage size. This allows designers to tailor the memory to meet the algorithm requirements.

TDM Mode

TDM (Time Division Multiplexed) mode refers to time division multiplexing which is a common mode for transferring serial data. In telecommunications applications, T1 and E1 lines use TDM. TDM allows multiple serial devices to send and receive information using the same physical connection. TDM also allows communication between multiple DSPs.

All ADI products support TDM mode in the serial ports.

Zero-Overhead Looping

The code for most DSP routines falls naturally into a set of nested loops. Without the support for zero-overhead looping, the DSP core must spend cycles calculating the loop termination values, in addition to the cycles used to process the algorithm's computations. Without zero-overhead looping, performance degrades.

ADI offers 16-bit fixed-point and 32-bit fixed/floating-point DSPs with zero overhead, nestable looping to save instruction cycles.

ADI Processor Benchmarks*

Blackfin Processor Benchmarks	Cycle Count	Execution Time @ 600 MHz
Block FIR Filter	h/2	
Biquad IIR Filter (4 coeff)	2.5*bq	
Complex FIR Filter	2*h	
Delayed LMS Filter	1.5h	
1024-Point Complex FFT (prescaled)	13938	23 us
256-Point Complex FFT (out-of-place)	3610	6 us
Max Search	x/2	
Max Index Search	x/2	
TigerSHARC Processor Benchmarks	**Cycle Count**	**Execution Time @ 300 MHz**
1024-Point Complex Radix-2 FFT (32-bit Float)	9835	32.78 us
256-Point Complex Radix-2 FFT (16-bit)	1100	3.67 us
50 Tap FIR Filter on 1024 Point Input (16-bit)	7200	24 us
Single Complex FIR MAC (16-bit)	0.5	.00167 us
Vector Dot Product for 7200 Point Input (16-bit)	890	2.98 us
SHARC DSP Benchmarks	**ADSP-21065L**	**ADSP-21161N**
Clock Speed	66 MHz	100 MHz
Instruction Cycle Time	15 ns	10 ns
MFLOPS Sustained, Peak	132, 198 MFLOPS	400, 600 MFLOPS
MOPS (32-bit Fixed-Point) Sustained, Peak	132, 198 MFLOPS	400, 600 MFLOPS
1024-Point Complex FFT (Radix 4, with Digit Reverse)	0.27 ms (SISD)	0.17 ms
FIR Filter (per Tap)	15 ns	5 ns
IIR Filter (per Biquad)	60 ns	40 ns **
Matrix Multiply		
(3x3) x (3x1)	135 ns	30 ns
(4x4) x (4x1)	240 ns	37 ns
Divide (y/x)	90 ns	60 ns **
Inverse Square Root	135 ns	90 ns **

* Benchmarks are for best data conditions

** Specified in SISD mode. Using SIMD, the same benchmark applies for 2 sets of computations. For example, 2 sets of biquad operations can be performed in the same amount of time as the SISD mode benchmark.

h = # of taps
bq = # of biquads
x = # of samples

BDTImark2000™ Scores

Fixed Point	
ADSP-BF533 (600 MHz)	3280
ADSP-BF535 (300 MHz)	1690
ADSP-219x (160 MHz)	420
ADSP-218x (80 MHz)	240
Floating Point	
ADSP-2116x (100 MHz)	510
ADSP-2106x (66 MHz)	250

The BDTImark2000™ provides a summary measure of DSPspeed. Ahigher score indicates a faster processor. For more information and scores, visit www.BDTI.com.

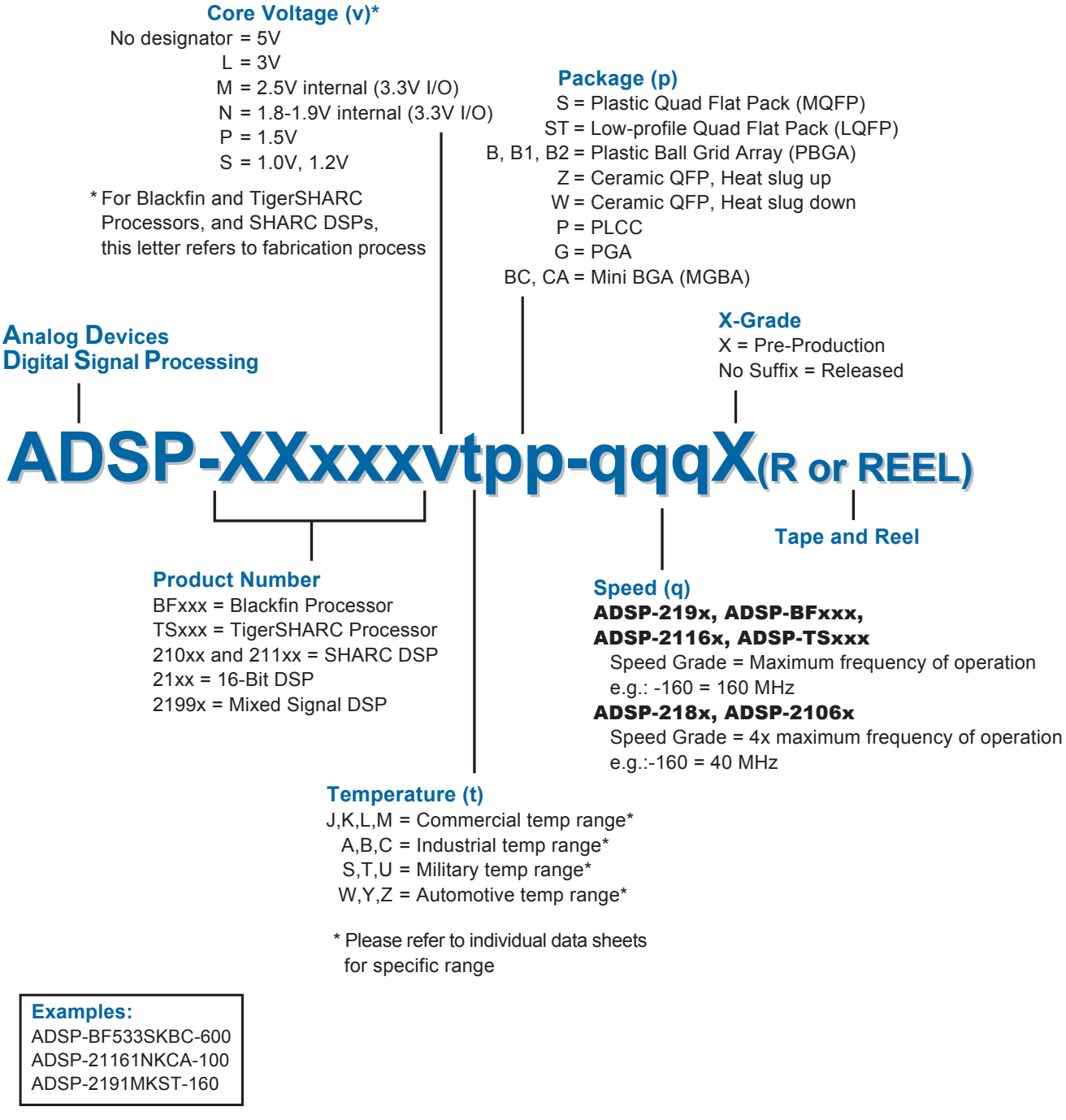
ADI Processor Benchmarks*

ADSP-219x/ADSP-2199x Benchmarks	Cycle Count	Execution Time @ 160 MHz
FIR Filter [2]	h	
Biquad IIR Filter [1,2]	5*bq	
Complex FIR Filter [2]	4*(h-1)	
1024-Point Complex FFT Radix 2 [3]	22105	138 us
256-Point Complex FFT Radix 2 [3]	5342	33 us
Division	19	119 ns
Sin/Cos [4]	11	69 ns
Arc Tangent [4]	13	81 ns
Ln/log10 [4]	11	69 ns
ADSP-218x Benchmarks	**Cycle Count**	**Execution Time @ 80 MHz**
FIR Filter [3]	h	
Biquad IIR Filter [1,2]	5*bq	
Complex FIR Filter [2]	4*(h-1)	
1024-Point Complex FFT Radix 4 [3]	37021	465 us
256-Point Complex FFT Radix 4 [3]	7372	93 us
Division	19	238 ns
Sin/Cos [4]	11	313 ns
Arc Tangent [4]	13	163 ns
Ln/log10 [4]	11	138 ns
Square Root	23	288 ns

[1] Assumes 4-coefficients (a0, b0 normalized)
[2] Per tap/biquad
[3] Input scaling, worst case includes bit reversal
[4] Assumes redundant bits have been removed

* Benchmarks are for best data conditions

Part Numbering System



Examples:
ADSP-BF533SKBC-600
ADSP-21161NKCA-100
ADSP-2191MKST-160

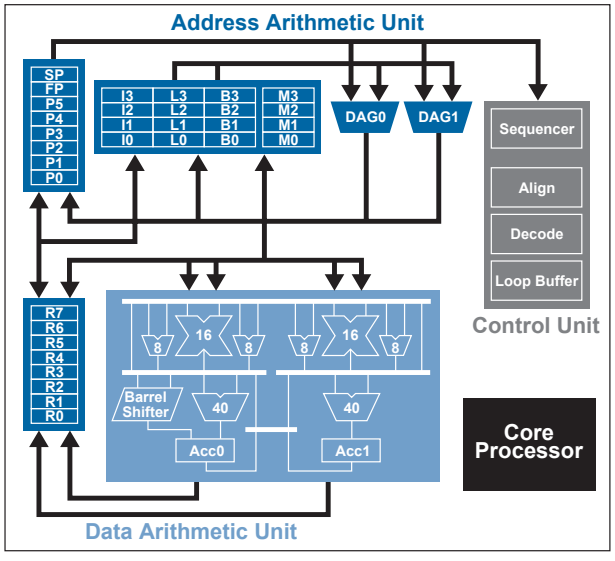
Blackfin® Processor Family
High Performance, Low Power, Processing Leadership

Blackfin Processors are a new breed of embedded media processor designed specifically to meet the computational demands and power constraints of today's embedded audio, video and communications applications. Based on the Micro Signal Architecture (MSA) jointly developed with Intel Corporation, Blackfin Processors combine a 32-bit RISC-like instruction set and dual 16-bit multiply accumulate (MAC) DSP functionality with the ease-of-use attributes found in general-purpose microcontrollers. This combination of processing attributes enable Blackfin Processors to perform equally well in both signal processing and control processing applications—in many cases deleting the requirement for separate heterogeneous processors.

Currently, Blackfin Processors offer performance to 600MHz/1,200 MMACs with a roadmap to 1GHz. The Blackfin Processor family also offers industry leading power consumption performance to as low as 0.15mW/MMAC at 0.7V.

High Performance Signal Processing

The Blackfin Processor architecture employs numerous techniques to ensure that signal processing performance is maximized. These include a fully interlocked instruction pipeline, multiple parallel computational blocks, efficient DMA capability, and instruction set enhancements designed to accelerate video processing.



Fully Interlocked Instruction Pipeline

All Blackfin Processors utilize a multi-stage fully interlocked pipeline that guarantees code is executed as you would expect and that all data hazards are hidden from the programmer. This type of pipeline guarantees result accuracy by stalling when necessary to achieve proper results. This greatly simplifies the programming task since the software engineer doesn't have to completely understand pipeline latency issues. On-chip interlocking hardware ensures that operand data is valid at the time of a particular instruction's execution. The VisualDSP++ development tools support this superpipelined architecture by incorporating a pipeline viewer screen that shows an instruction's execution status and highlights potential pipeline stalls.

Highly Parallel Computational Blocks

Computational blocks within the architecture are designed to maximize the number of mathematical operations that can execute within any given clock cycle. The basis of the Blackfin Processor architecture is the Data Arithmetic Unit that includes two 16-bit Multiplier Accumulators (MACs), two 40-bit Arithmetic Logic Units (ALUs), four 8-bit video ALUs, and a single 40-bit barrel shifter. Each MAC can perform a 16-bit by 16-bit multiply on four independent data operands every cycle. The 40-bit ALUs can accumulate either two 40-bit numbers or four 16-bit numbers. With this architecture, 8-, 16- and 32-bit data word sizes can be processed natively for maximum efficiency.

High Bandwidth DMA Capability

All Blackfin processors have multiple, independent DMA controllers that support automated data transfers with minimal overhead from the processor core. DMA transfers can occur between the internal memories and any of the many DMA-capable peripherals. Transfers can also occur between the peripherals and external devices connected to the external memory interfaces, including the SDRAM controller and the asynchronous memory controller.

Video Instructions

In addition to native support for 8-bit data, the word size common to red-green-blue pixel processing algorithms, the Blackfin Processor architecture includes instructions specifically defined to enhance performance in video processing applications. For example, the Discrete Cosine Transform (DCT) is supported with an IEEE 1180 rounding operation. The "SUM ABSOLUTE DIFFERENCE" instruction supports motion estimation algorithms used in video compression algorithms such as MPEG2, MPEG4, and JPEG.

Efficient Control Processing

The Blackfin Processor architecture also offers a variety of benefits most often seen in RISC control processors. These features include a hierarchical memory architecture, superior code density, and a variety of microcontoller-style peripherals including watch-dog timer, real-time clock, and an integrated SDRAM controller. All of these features provide the system designer with a great deal of design flexibility while minimizing end system costs.

Hierarchical Memory

The Blackfin Processor memory architecture provides for both Level 1 (L1) and Level 2 (L2) memory blocks in device implementations. The L1 memory is connected directly to the processor core, runs at full system clock speed, and offers maximum system performance for time critical algorithm segments. L1 memory can be configures as SRAM, cache, or a combination of both. The L2 memory is a larger, bulk memory storage block that offers slightly reduced performance.

The Memory Management Unit provides for a memory protection format that, when coupled with the core's User and Supervisor modes, can support a full OS Kernel. The OS Kernel runs in Supervisor mode and partitions blocks of memory and other system resources for the actual application software to run in User mode. This is a unique and powerful feature not present on traditional DSPs.

Superior Code Density

The Blackfin processor architecture supports multi-length instruction encoding. Very frequently used control-type instructions are encoded as compact 16-bit words with more mathematically intensive DSP instructions encoded as 32-bit values. The processor will intermix and link 16-bit control instructions with 32-bit DSP instructions into 64-bit groups to maximize memory packing. When caching and fetching instructions, the core automatically fully packs the length of the bus because it does not have alignment constraints. When combined, these two features enable Blackfin Processors to deliver code density benchmarks comparable to industry-leading RISC processors

Dynamic Power Management

All Blackfin Processors employ a number of power saving techniques for applications requiring minimal power consumption. Blackfin Processors are based on a gated clock core design that selectively powers down functional units on an instruction-by-instruction basis. Blackfin Processors also support multiple power-down modes for periods where little or no CPU activity is required. Lastly, and probably most importantly, Blackfin Processors support a dynamic power management scheme whereby the operating frequency AND voltage can be tailored to meet the performance requirements of the algorithm currently being executed. These transitions may occur hundreds of times per second under the control of an RTOS or user firmware. Currently available products also offer on-chip core voltage regulation circuitry as well as operation to as low as 0.7V and are particularly well suited portable applications requiring extended battery life.

Easy to Use

A single Blackfin Processor can be utilized in many applications previously requiring both a high performance signal processor and efficient control processor. This benefit greatly reduces development time and costs ultimately enabling end products to get to market sooner.

ADSP-BF535 Blackfin® Processor

High Performance Processor for Networking/Digital Imaging

The ADSP-BF535 combines a high performance processor, Dynamic Power Management, programming ease of use with a rich, powerful peripheral set in order to be the central element for a variety of application solutions with a minimum of external components and cost.

Features

- High-performance 350 MHz/700 MMAC dual-MAC processor core
- 308 KBytes of On-Chip Memory
  - 16 KBytes of L1 Program Memory
  - 36 KBytes of L1 Data Memory
  - 256 KBytes of Unified L2 Memory
- External Memory Controller with glueless support for synchronous and asynchronous memories
- Memory Management Unit providing memory protection
- 32-bit 33 MHz PCI V2.2 interface with both master and slave functionality
- USB Device V1.1 controller supporting up to 8 endpoints
- Two full-duplex Synchronous Serial ports (SPORTs)
- Three 32-bit timer/counters supporting PWM output and pulse width/event count input modes
- 12 channel peripheral and memory DMA controller capable of internal, external and PCI transfers
- Two UARTs with auto-baud capability (UART0 supports IrDA® functionality)
- Two SPI-compatible ports
- 16 General Purpose I/O
- PLL capable of 1x to 31x frequency multiplication
- Event controller
- Real-time clock
- Watchdog timer
- Debug/JTAG interface
- Commercial and industrial temperature range
- 260-Lead (19 mm x 19 mm) PBGA package

Benefits

- Single core integration of DSP and RISC functionalities eliminates the need for multiple processors
- Enhanced instructions enable highly efficient audio, image and video processing
- Flexible, software-controlled dynamic power management optimizes power consumption
- Optimized C/C++ programmability increases flexibility and shortens time to market
- Rich peripheral set expands users options for easy system integration

Applications

- Automotive applications
- Broadband home gateways
- Central office/network switch
- Digital imaging and printing
- Global positioning systems
- Home networking/wireless LAN
- Industrial signal processing
- Internet appliances
- Internet audio
- Modem solutions
- Private Branch Exchanges (PBX)
- Telecommunications
- Video conferencing
- VoIP phone solutions

Model	Max MMACS	L1/L2 Memory	Operating Voltage Core, I/O	Pin/Pkg	Price* (1000)
ADSP-BF535PKB-350	700	52KB/256KB	1.0-1.6V/3.3V	260-PBGA	$44.80
ADSP-BF535PBB-300	600	52KB/256KB	1.0-1.5V/3.3V	260-PBGA	$35.20
ADSP-BF535PKB-300	600	52KB/256KB	1.0-1.5V/3.3V	260-PBGA	$32.00
ADSP-BF535PBB-200	400	52KB/256KB	1.0-1.5V/3.3V	260-PBGA	$30.00

K = Commercial Temp (0ºC to +70ºC Ambient)
B = Industrial Temp (-40ºC to +85ºC Ambient)
* All pricing is budgetary – subject to change

ADSP-BF531/2/3 Blackfin® Processors

Low Cost, Fixed-Point Processors for Multimedia/Communications

The enhanced Blackfin Processor family offers a pin- and code-compatible path to industry-leading performance, power consumption, and price points. Offering performance levels of 1200MMACs and product derivatives as low as US$5 (in 10K quantities), the Blackfin Processor architecture is capable of satisfying the ever-increasing requirements of the most demanding signal processing markets and applications. Combining these features with an easy-to-use RISC-like Instruction Set Architecture and application-tuned system peripherals, Blackfin Processors enable a unique design experience that ensures product time to market is minimized.

The three new family members of the Blackfin Processor family– the ADSP-BF533, ADSP-BF532, and ADSP-BF531 – offer significantly higher performance and lower power than first generation Blackfin Processors. Differing solely with respect to their performance and on-chip memory, the three new processors are completely pin-compatible, thus mitigating many risks associated with new product development.

The enhanced Blackfin Processor series offers:

- Performance to 600MHz/1200MMACs enabling multi-channel audio plus VGA/D1 video processing in multimedia applications
- Enhanced Dynamic Power Management capabilities enabling device operation to 0.7V for extending battery life in portable applications
- Application-tuned peripherals providing glueless connectivity to general purpose convert ers in data acquisition applications
- Multiple low-cost, pin- and code-compatible derivatives enabling software differentiation in cost-sensitive consumer applications.

Digital Media Processing

Video and imaging data have become the world's primary communication mechanisms. Digital video is being used increasingly for applications such as digital still cameras and camcorders, home entertainment, automotive safety, and security/ surveillance. Blackfin Processor features greatly simplify hardware design while decreasing the overall system bill of materials costs in digital media products.

Enhanced Blackfin Processors:

- Combine video-specific core features/instructions with 600MHz operating speeds, enabling the processor to implement VGA/D1 resolution video encoders/decoders including MPEG2, MPEG4, Windows Media Video, and H.264.
- Utilize a programmable core architecture that cuts time-to-market by enabling quick transitions between multiple evolving and competing still image and video compression standards.
- Offer glue-less connectivity via a Parallel Peripheral Interface to ITU-R 656 video encoders, decoders, and CMOS image sensors.
- Include integrated serial ports to support I²S audio framing, prevalent in consumer media applications.

Portable Information Appliances

Portable Information Appliances are highly dependent on battery power. Therefore, minimizing power consumption, which directly impacts battery life, is extremely important. All Blackfin Processors include a Dynamic Power Management (DPM) subsystem that can decrease the core voltage and operating frequency to save power during non-time-critical operations.

Additionally, multiple power-down modes that selectively turn off power to non-essential silicon components are supported. These power-saving features, when combined with a high performance core and flexible interfaces to A/D converters, also make enhanced Blackfin Processors particularly well suited for Point-of-Sales terminals, portable test equipment, and medical/industrial instruments.

Automotive Telematics and Infotainment

The basic core architecture of enhanced Blackfin Processors is particularly efficient for combined signal processing and control processing scenarios such as automotive telematics and infotainment. The dual 16-bit MAC architecture provides 1200MMACs of sustained signal processing performance – sufficient for the most demanding applications, such as noise/echo cancellation, audio and video decompression, and speech recognition.

ADSP-BF531/2/3 Blackfin® Processors

Low Cost, Fixed-Point Processors for Multimedia/Communications

Blackfin processors also offer benefits more generally associated with RISC processors – specifically, a very orthogonal instruction set, byte addressability, memory protection, and an SRAM/Cache memory model. The peripheral set of enhanced Blackfin Processors not only reduces the overall system costs in telematics systems, but also provides a glueless communication mechanism between the multiple telematics subsystems – GPS, cellular terminal, CD, DVD, and possibly Bluetooth wireless.

Features

- High-performance 600 MHz/1200 MMAC dual-MAC core
- Up to 148 KBytes of on-chip L1 memory
  - 80 KBytes Program SRAM/Cache
  - 64 KBytes Data SRAM/Cache
  - 32 KBytes Program ROM (ADSP-BF531/BF532 only)
- Parallel Peripheral Interface supporting ITU-R 656 video data formats
- Two dual-channel, full-duplex Synchronous Serial Ports (SPORTs) supporting eight stereo I²S channels
- 12 DMA channels supporting one and two-dimensional data transfers
- Memory controller providing glueless connection to multiple banks of external SDRAM, SRAM, Flash, or ROM
- Three timer/counters supporting PWM and pulse width/event count modes
- UART with support for IrDA®
- SPI-compatible port
- PLLcapable of 1x to 63x frequency multiplication
- Event handler
- Real-time clock
- Watchdog timer
- On-chip core voltage regulator
- 160-lead (12 mm x 12 mm) mini-BGA package, and 176-lead (24 mm x 24 mm) LQFPpackage
- Industrial and commercial temperature ranges

Benefits

- Performance to 600MHz enables multi-channel audio plus VGA/D1 video processing in multimedia applications
- Single core integration of DSP and RISC functionalities eliminates the need for multiple processors
- Enhanced instructions enable highly efficient audio, image and video processing
- Flexible, software-controlled dynamic power management with on-chip voltage regulator optimizes power consumption, increasing battery life time of portable devices
- Application-tuned peripherals enable glueless system integration to audio, video, and general purpose converters
- Multiple low cost, pin- and code-compatible derivatives enable software differentiation in cost sensitive consumer applications
- Optimized C/C++ programmability increases flexibility and shortens time to market
- User definable ROM option minimizes system costs

Applications

- Automotive safety systems
- Biometrics
- Broadband wireless
- Consumer multimedia
- Digital network media devices
- Digital radio
- Embedded modems
- Information appliances
- Portable media players
- Portable test equipment
- POS terminals
- Security and surveillance
- Telephony and communications
- VOIP

Model	Max MMACS	L1 Memory	Operating Voltage Core, I/O	Pin/Pkg	Price/1K
ADSP-BF533SKBC-600	1200	148KB	0.7-1.2V/3.3V	160-MBGA	$23.50
ADSP-BF533SBBC-500	1000	148KB	0.7-1.2V/3.3V	160-MBGA	$20.00
ADSP-BF532SBBC-400	800	116KB*	0.7-1.2V/3.3V	160-MBGA	$11.50
ADSP-BF532SBST-300	600	116KB*	0.7-1.2V/3.3V	176-LQFP	$11.50
ADSP-BF531SBBC-400	800	84KB*	0.7-1.2V/3.3V	160-MBGA	$8.00
ADSP-BF531SBST-300	600	84KB*	0.7-1.2V/3.3V	176-LQFP	$7.00

* Includes 32KB of user-definable ROM

K = Commercial Temp (0ºC to +70ºC Ambient)
B = Industrial Temp (-40ºC to +85ºC Ambient)
* All pricing is budgetary – subject to change

TigerSHARC® Processor Family
Highest Performance Processor for Multiprocessor Systems

Analog Devices' TigerSHARC processors offer the best-in-class performance in terms of MACs and FLOPS delivered per watt, per dollar and per square inch of PCB space. The processors embody a breakthrough static superscalar architecture that boasts native support of 1-, 8-, 16-, and 32-bit fixed-point and floating-point data types on a single chip. TigerSHARC processors are well-suited to numerous signal processing applications that rely on multiple processors working together to execute computationally-intensive real-time functions.

High Performance

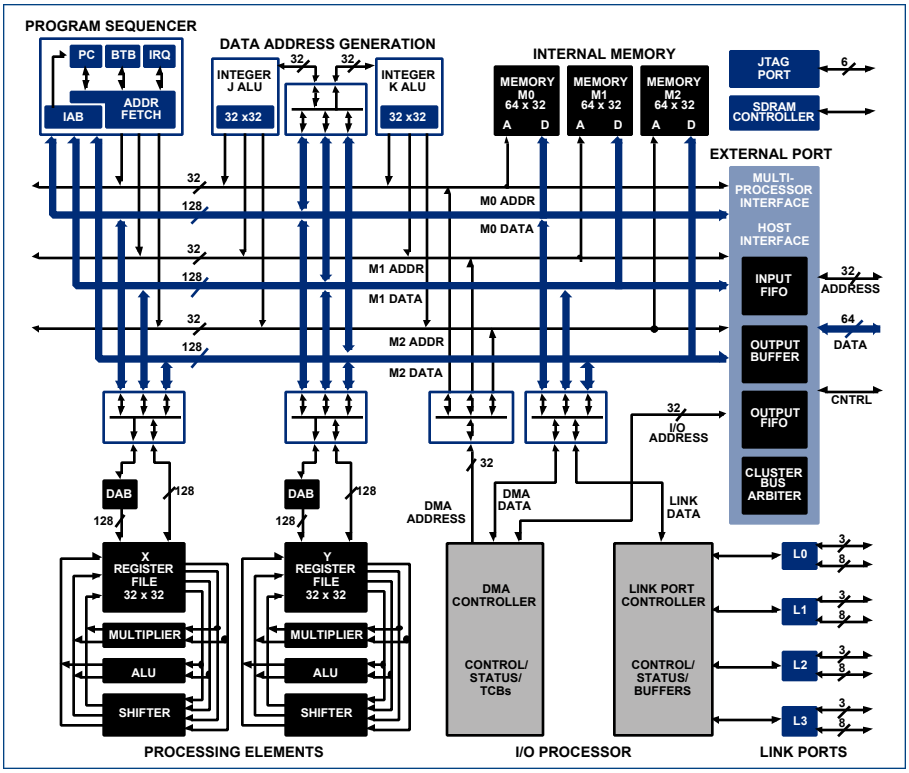
Offering the world's fastest floating-point performance, TigerSHARC Processors are optimized for applications that demand the highest signal processing performance such as wireless infrastructure, industrial, digital broadcast systems, video, telephony, military, medical equipment, imaging, and pattern recognition.

Optimized for Multiprocessing Needs

TigerSHARC processors offer two types of integrated multiprocessing support (link ports and a cluster bus) that enable glueless scalability and unmatched I/O performance. This means TigerSHARC processors will gluelessly scale up to 8 devices on the cluster with global memory. Four on-chip link ports provide a high bandwidth point-to-point connection that is complementary to the cluster multiprocessing.

Multiple Data Types Allow Increased Flexibility

The ADSP-TS101S TigerSHARC processor is an ultra-high performance, static superscalar processor optimized for large signal processing tasks and communications infrastructure. The processors combines very wide memory widths with dual computation blocks – supporting 32-bit and 40-bit floating-point and supporting 1-, 8-, 16-, and 32-bit fixed-point processing that allows the user flexibility to select the appropriate data type.



ADSP-TS101

Highest Performance Fixed-and Floating-Point Multiprocessor

At a 300 MHz clock rate, the ADSP-TS101S offers the highest fixed-and floating-point signal processing performance available. The ADSP-TS101S TigerSHARC® processor operates at an industry-leading 2.4 billion multiply accumulates per second (GMACS) and 1.8 billion floating-point operations per second (GFLOPS) as well as a 32-bit floating-point 1024 complex FFT time of 32.9 microseconds.

Targeted at numerous signal processing applications that rely on multiple processors working together to execute computationally-intensive real-time functions, the ADSP-TS101S is well-suited to video and communication markets, including the 3G cellular and broadband wireless base stations, as well as defense, medical imaging, industrial instrumentation.

Features

- 2.4 billion 16-bit MACs-per-second
- 950 MFLOP/watt – industry best
- 1.2 volt supply with 3.3 volt I/O
- 3.2 ns instruction cycle time at 300 MHz
- Eight 16-bit MACs/cycle with 40-bit accumulation
- Two 32-bit MACs/cycle with 80-bit accumulation
- 6 Mbit on-chip SRAM
- IEEE floating-point compatible
- 14 DMA channels
- 4 Link ports – 1 GByte/sec transfer rate, aggregate
- 32/64-bit external port – 800 MBytes/sec
- 128 general purpose registers
- Optimizing C/C++ compiler
- Glueless multiprocessing
- 19 x 19 mm or 27 x 27 mm PBGA

Benefits

- Integrated multiprocessing features make building scalable systems easy
- Support for multiple data formats in hardware provides high flexibility and efficiency
- Specialized instructions increase performance for telecommunications applications

Applications

- Basestations (2G, 2.5G, 3G)
- Medical, CT, ultrasound
- Sonar and radar systems
- Flight simulator
- Infrastructure equipment
- Military smart munitions
- Test equipment
- Imaging, printers
- Wireless broadband access
- Industrial applications

Development Tools	
ADDS-TS101S-EZLITE	Evaluation Kit
VDSP-TS-PC-FULL	VisualDSP++
VDSP-TS-PCFLOAT	VisualDSP++ Floating License
ADDS-APEX-ICE	USB-Based Emulator
ADDS-HPPCI-ICE	PCI-Based Emulator

Model	MHz	On-Chip Memory	Operating Voltage Core, I/O	Pin/Pkg	Price* (1000)
ADSP-TS101SAB1-000	250	6 Mbits	1.2V/3.3V	625-PBGA	$207.00
ADSP-TS101SAB2-000	250	6 Mbits	1.2V/3.3V	484-PBGA	$207.00
ADSP-TS101SAB1-100	300	6 Mbits	1.2V/3.3V	625-PBGA	$234.00
ADSP-TS101SAB2-100	300	6 Mbits	1.2V/3.3V	484-PBGA	$234.00

A = Industrial Temp (-40ºC to +85ºC Case)
* All pricing is budgetary – subject to change

SHARC® DSP Family
Leadership in Premium Audio Applications

Analog Devices' "Super" Harvard architecture SHARC DSP family is optimized to enable a variety of real-time embedded signal processing applications. The unique memory architecture – two large on-chip, dual-ported SRAM blocks coupled with the sophisticated I/O processor – enables the SHARC to sustained high-speed computational requirements of today's applications. Performance is predictably high and sustained – just as it should be for real-time embedded DSP development.

SHARC DSPs deliver high performance and code compatibility within more than 50 products. One architecture powers applications, from mainstream to multiprocessing, with DSPs that can execute 5 billion operations per second with a price range as low as $10. Code-compatibility across the family helps to keep development time to a minimum, and maximize our customers' software investments.

The popularity of SHARC DSPs is evident in our leadership in multiprocessing applications. Patented link port technology has helped establish SHARC as a de facto standard. Future generations of this high-performance family of DSPs will continue to deliver performances needed in a single-chip solution as well as maintain the multiprocessing leadership enabled by clusters of versatile SHARC DSPs.

Applications

- AVR/home theater audio
- Automotive audio
- Prosumer audio
- Professional audio
- Instrumentation
- Medical imaging
- Radar and sonar guidance
- Engine control

32-BIT Generic	Max MIPS	On-Chip Memory	Operating Voltage Core, I/O	Pin/Pkg	Serial Ports	Price* (1000)
ADSP-21161N	100	1 Mbit	1.8V/3.3V	225-PBGA	4	$24.63
ADSP-21160N	100	4 Mbits	1.9V/3.3V	400-PBGA	2	$145.00
ADSP-21160M	80	4 Mbits	2.5V/3.3V	400-MBGA	2	$145.00
ADSP-21065L	66	544 Kbits	3.3V/3.3V	208-MQFP/196-MBGA	2	$19.50
ADSP-21061/L	50	1 Mbit	3.3V/5V	225-PBGA	2	$37.43
ADSP-21060/L	40	4 Mbits	3.3V/5V	240-MQFP/225-PBGA	2	$249.29
ADSP-21062/L	40	2 Mbits	3.3V/5V	240-MQFP/225-PBGA	2	$100.00

Package: PBGA = Plastic Ball Grid Array MBGA = Mini Ball Grid Array
PQFP = Plastic Quad Flat Pack

* US Dollars. Lowest grade suggested resale price per unit in 1000 unit quantities
All pricing is budgetary - subject to change

ADSP-21161N

Low-Cost, Single-Instruction, Multiple-Data (SIMD) SHARC®

The ADSP-21161N is the newest member of the high performing SIMD SHARC DSP family. This device offers 32-bit floating-point DSP performance at a price that will support consumer applications.

Features

- 3.3 Volt external/1.8 volt internal
- 1 Mbit on-chip SRAM
- 14 zero-overhead DMA channels
- SPI-compatible port for serial host and peripheral control
- 4 SPORTs supporting 128 channel TDM and I²S
- 12 general purpose I/O lines, 4 IRQ lines,1 timer
- Code-compatible to all other SHARC family DSPs
- Single-Instruction, Multiple-Data (SIMD) computational architecture – two 32-bit IEEE floating-point computation units, each with a multiplier, ALU, shifter, and register file
- 100 MHz (10 ns) core instruction rate 600 MFLOPS peak and 400 MFLOPs sustained performance
- Dual Data Address Generators (DAGs) with modulo and bit-reverse addressing
- Zero-overhead looping with single-cycle loop setup, providing efficient program sequencing
- IEEE 1149.1 JTAG standard test access port and on-chip emulation
- 225-ball 17 mm x 17 mm PBGA package

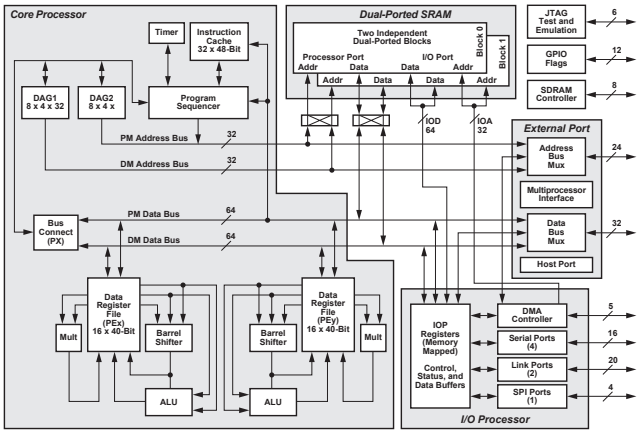
Development Tools	
ADDS-21161N-EZLITE	Evaluation Kit
VDSP-SHARC-PC-FULL	VisualDSP++
VDSP-SHARC-PCFLOAT	VisualDSP++ Floating License
ADDS-APEX-ICE	USB-Based Emulator
ADDS-HPPCI-ICE	PCI-Based Emulator

Benefits

- Cluster multiprocessing and two 100 Mbyte/s link ports simplify connection and communication for multiprocessing
- SDRAM controller improves large DRAM bank throughput
- 4 serial ports allow 16 channels of data to be transferred in/out of the DSP

Applications

- High-end consumer and professional audio
- Automotive audio
- Adaptive cruise control and collison avoidance
- Medical equipment
- Test equipment
- Speech recognition
- Finger print recognition
- Multi access motor control
- Power line modems and telephony



Model	MHz	On-Chip Memory	Operating Voltage Core, I/O	Pin/Pkg	Price* (1000)
ADSP-21161NKCA-100	100	1 Mbit	1.8V/3.3V	225-MBGA	$24.63
ADSP-21161NCCA-100	100	1 Mbit	1.8V/3.3V	225-MBGA	$29.55

K = Commercial Temp (0ºC to +85ºC case)
C = Industrial Temp (-40ºC to +105ºC case)
* All pricing is budgetary – subject to change

ADSP-21160
Single-Instruction, Multiple-Data (SIMD) SHARC®

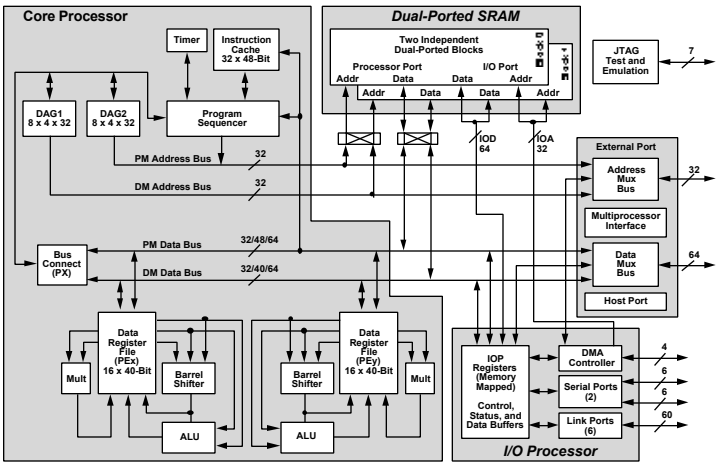
Features

- 600 MFLOPS (32-bit floating-point) peak operation
- 600 MOPS (32-bit fixed-point) peak operation
- 100 MHz core operation, 10 ns cycle time
- 92 µs 1024-point complex FFT benchmark with bit reversal
- Code compatible with first generation SHARC
- SIMD core includes 2 multipliers, 2 ALUs, 2 shifters, and 2 register files
- 4 Mbits on-chip dual-ported SRAM
- Division of SRAM between program and data memory is selectable
- Core can fetch four 32-bit words from memory in a single processor cycle using two 64-bit wide buses
- Dual data address generators with modulo and bit-reverse addressing
- Efficient program sequencing with zero-overhead looping—single-cycle loop setup
- IEEE JTAG standard 1149.1 test access port and on-chip emulation
- 32-bit single-precision IEEE floating-point data type and 40-bit extended precision floating-point data type support
- 32-bit fixed-point formats, integer and fractional, with 80-bit accumulators in both processing elements
- 14 channels of zero-overhead DMA
- Glueless connection for scaleable DSP multiprocessing architectures
- Distributed on-chip bus arbitration for parallel bus connect of up to six ADSP-21160s plus host
- Six 100 Mbytes/sec link ports for point-to-point connectivity and array multi-processing
- 2.5 volt core, 3.3 volt I/O (80 MHz ADSP-21160M)

Applications

- Instrumentation/industrial
- High-end audio
- Radar and sonar
- Imaging
- Speech recognition
- 3D graphics acceleration for workstations and arcade video games

Development Tools	
ADDS-21160-EZLITE	Evaluation Kit for “M”
ADDS-21160N-EZLITE	Evaluation Kit for “N”
VDSP-SHARC-PC-FULL	VisualDSP++
VDSP-SHARC-PCFLOAT	VisualDSP++ Floating License
ADDS-APEX-ICE	USB-Based Emulator
ADDS-HPPCI-ICE	PCI-Based Emulator



Model	MHz	On-Chip Memory	Operating Voltage Core, I/O	Pin/Pkg	Price* (1000)
ADSP-21160MKB-80	80	4 Mbits	2.5V/3.3V	400-PBGA	$145.00
ADSP-21160NKB-100	100	4 Mbits	1.9V/3.3V	400-PBGA	$145.00

K = Commercial Temp (0ºC to +85ºC case)
* All pricing is budgetary – subject to change

ADSP-21065L
Low-Cost Entry-Point to the SHARC® DSP Family

Features

- 544 KBits configurable dual-ported on-chip memory
- 64M x 32-bit word external address space
- 198 MFLOPS (32-bit floating-point)
- 198 MOPS (32-bit fixed-point)
- Glueless SDRAM interface
- 2 serial transmit/receive ports support 32-channel TDM
- I²S mode supports up to 16 channels
- 2 timers with event capture and PWM options
- 12 programmable I/O pins
- 10 DMA channels
- Glueless multiprocessing with 2 ADSP-21065L's
- Code compatible with all SHARC family members
- 3.3 volt, 208-pin MQFP, 196 MBGA

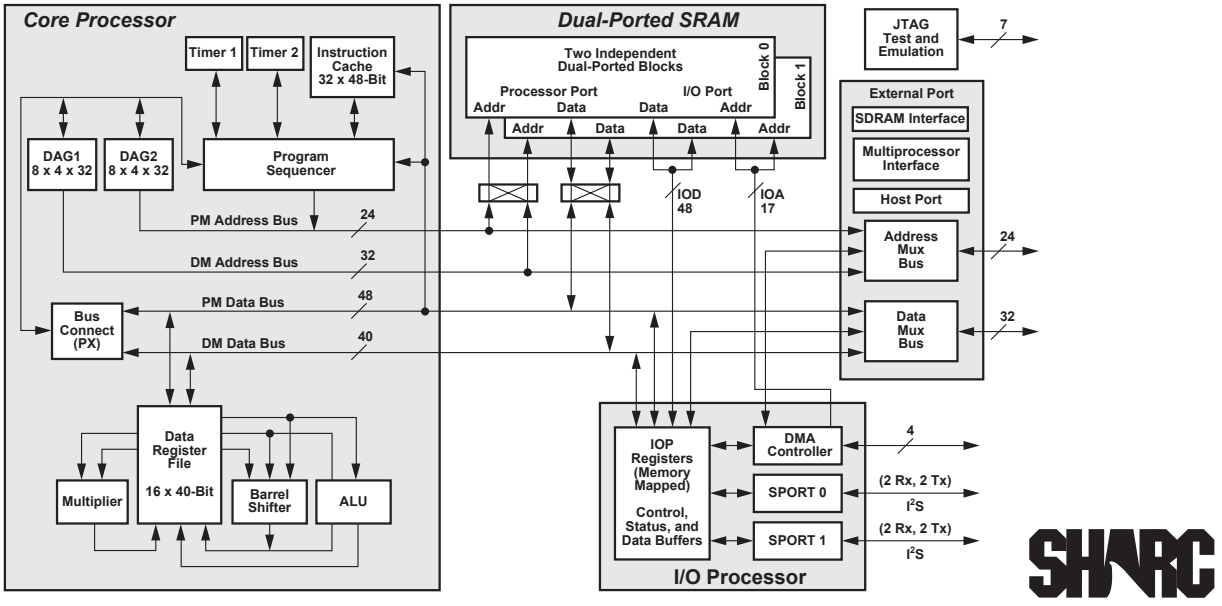
Applications

- Digital audio
- Keyless entry using voice analysis/recognition
- Bar code scanners
- Imaging
- Ultrasound equipment
- Digital oscilloscopes
- Fingerprint recognition

Development Tools	
ADDS-21065L-EZLITE	Evaluation Kit
VDSP-SHARC-PC-FULL	VisualDSP++
VDSP-SHARC-PCFLOAT	VisualDSP++ Floating License
ADDS-APEX-ICE	USB-Based Emulator
ADDS-HPPCI-ICE	PCI-Based Emulator

Model	MHz	On-Chip Memory	Operating Voltage Core, I/O	Pin/Pkg	Price* (1000)
ADSP-21065LKS-240*	60	544 Kbits	3.3V/3.3V	208-MQFP	$19.50
ADSP-21065LKS-264	66	544 Kbits	3.3V/3.3V	208-MQFP	$37.50
ADSP-21065LKCA-240	60	544 Kbits	3.3V/3.3V	196-MBGA	$38.00
ADSP-21065LKCA-264	66	544 Kbits	3.3V/3.3V	196-MBGA	$39.50
ADSP-21065LCS-240	60	544 Kbits	3.3V/3.3V	208-MQFP	$37.50

L Indicates 3.3 Volt Operation
K = Commercial Temp (0ºC to +85ºC case)
C = Industrial Temp (-40ºC to +100ºC case)
*All pricing is budgetary – subject to change



SHARC

ADSP-2100 Architecture
Code-Compatible DSP Excellence

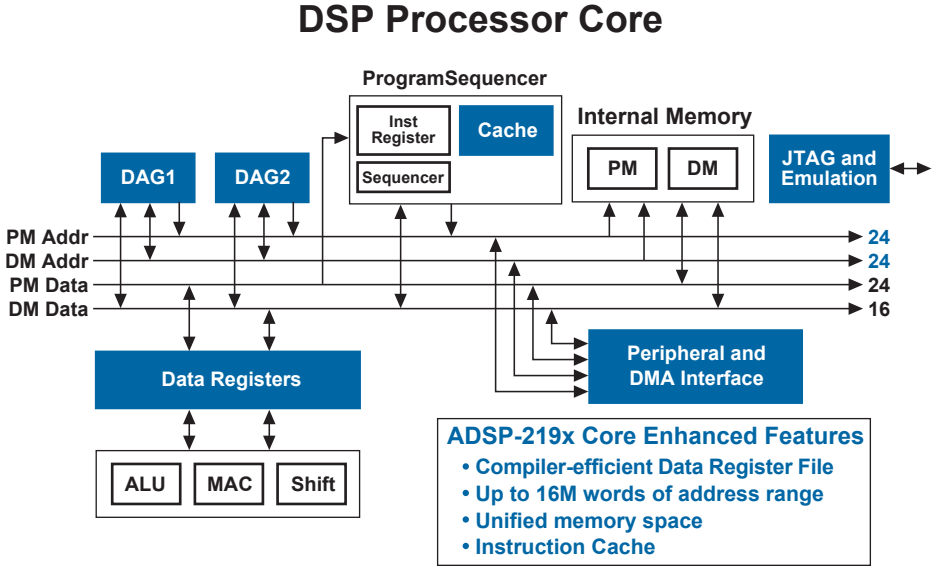
The ADSP-2100 family architecture is built around a common instruction set architecture (ISA) which is optimized for signal processing. All instructions are executed in a single clock cycle, including multi-function instructions. The architecture also features a high level algebraic programming syntax.

In addition, ADSP-21xx processors operate on 24-bit instructions and 16-bit data. The wider instruction word allows the device to use a more complex and robust instruction set than a 16-bit opcode. The 16-bit data word provides wide dynamic range, while the narrower bus width (16-bit as opposed to 32- or 64-bit wide) reduces power consumption.

Processors are available with up to 2.4 Mbits of SRAM around the DSP core to increase code execution and overall system performance. All ADSP-21xx processors integrate a programmable DMA controller to support maximum I/O throughput and processor efficiency. The ADSP-218x supports up to 4 Mbytes of external memory while the ADSP-219x architecture increases its address bus to 24-bits to support a total of 16M words of external memory. The ADSP-219x also balances a high performance processor core with high performance buses (PM, DM, DMA). It also provides two 40-bit accumulators and a 40-bit shifter, which help minimize data overflow during complex operations.

Addressing modes

ADSP-21xx processors also support immediate, register-direct, memory-direct, and register-indirect addressing modes. The ADSP-219x adds register, indirect-post-modify, immediate-modify, and direct- and indirect-offset addressing modes. Each address generator supports as many as four circular buffers, each with three registers. The ADSP-219x supports as many as 16 circular buffers using a DAG shadow register set and a set of base registers for additional circular-buffering flexibility.



ADSP-2100 Architecture
Code-Compatible DSP Excellence

Special Instructions

The ADSP-2100 architecture contains dedicated loop hardware and a “DO UNTIL” loop instruction that supports loops ranging from zero to 16K iterations, or loops with infinite iterations. The ADSP-218x supports up to four-deep nesting via its loop hardware and the ADSP-219x supports as many as eight. In addition to the standard arithmetic and logic instructions, the ALU (arithmetic-logic unit) supports division primitives. The ADSP-219x program sequencer features a 6-deep pipeline, and supports delayed branching. The ADSP-219x buses and instruction cache also provide rapid, unimpeded data flow to the core to maintain the high execution rate.

Compiler Friendly

Many of the enhancements to the ADSP-219x architecture were made to improve compiler efficiency. More flexible DAG addressing modes, added secondary DAG register, increased depth to stacks, and extended address reach to 16M words drastically improves compiler code efficiency.

ADSP-219x Family
160 MHz DSPs for Telephony and Signal Processing

The ADSP-219x series represent ADI's newest generation of ADSP-2100 code-compatible, fixed-point DSPs operating at 160 MHz. DSPs in this series integrate a high level of system interfaces to provide DSP developers with a rapid upgrade path to higher performance and lower system cost. The ADSP-219x DSP peripheral set has been optimized for Telephony applications by integrating three multi-channel serial ports that support up to 128 TDM channels, a 16-bit parallel and 16-bit host interface – this enables rapid deployment of cost effective voice platforms. The DSPs integrate up to 32K words of 24-bit program memory RAM, 32K words of 16-bit data memory RAM, and 16K words of 24-bit ROM. The ADSP-2191, ADSP-2195, and ADSP-2196 are all pin-compatible allowing many possibilities for system upgrades. Pin-to-pin compatibility allows programmers to migrate to larger memory models to increase end-product functionality without hardware redesign.

Features

- 160 MHz / MIPs 16-bit performance
- Up to 64K words on-chip SRAM
- 16K words on-chip ROM
- Boot ROM
- 16-bit external memory interface
- Host port interface (8- or 16-bit)
- Three full duplex multi channel TDM serial ports
- Two SPI interfaces
- One UART
- Three general purpose timers with PWM and input capture modes
- 16 general purpose I/O pins
- 11 DMA channels
- On-chip PLL with 1x to 32x input frequency multiplication
- IEEE JTAG 1149.1 test access port
- 2.5 volt supply with 3.3 volt I/O
- 144-Lead LQFP, 144-Lead mini-BGA

Benefits

- Programmable PLL with oscillator enables full speed operation from low-speed input clocks or crystals
- User selectable power-down modes reduces system power consumption
- On-chip ROM with application specific user code lowers cost in high volume systems
- Up to 11 DMA channels operate in parallel maximizes I/O throughput
- Efficient C/C++ compiler simplifies software programming task

Applications

- Telephony
- Modems
- Private Branch Exchange (PBX)
- Voice over network
- Home gateways
- Integrated access devices
- Optical networking
- Data acquisition
- Industrial automation

Model	MHz	Memory Words			Operating Voltage Core, I/O	Pin/Pkg	Price* (1000)
		DM RAM	PM RAM	PM ROM			
ADSP-2191MKST-160	160	32K	32K	–	2.5V/3.3V	144-LQFP	$16.85
ADSP-2191MBST-140	140	32K	32K	–	2.5V/3.3V	144-LQFP	$16.85
ADSP-2191MKCA-160	160	32K	32K	–	2.5V/3.3V	144-MBGA	$16.85
ADSP-2191MBCA-140	140	32K	32K	–	2.5V/3.3V	144-MBGA	$16.85
ADSP-2195MKST-160	160	16K	16K	16K	2.5V/3.3V	144-LQFP	$13.90
ADSP-2195MBST-140	140	16K	16K	16K	2.5V/3.3V	144-LQFP	$13.90
ADSP-2195MKCA-160	160	16K	16K	16K	2.5V/3.3V	144-MBGA	$13.90
ADSP-2195MBCA-140	140	16K	16K	16K	2.5V/3.3V	144-MBGA	$13.90
ADSP-2196MKST-160	160	8K	8K	16K	2.5V/3.3V	144-LQFP	$11.10
ADSP-2196MBST-140	140	8K	8K	16K	2.5V/3.3V	144-LQFP	$11.10
ADSP-2196MKCA-160	160	8K	8K	16K	2.5V/3.3V	144-MBGA	$11.10
ADSP-2196MBCA-140	140	8K	8K	16K	2.5V/3.3V	144-MBGA	$11.10

K = Commercial Temp (0ºC to +70ºC ambient)
B = Industrial Temp (-40ºC to +85ºC ambient)
* All pricing is budgetary – subject to change

ADSP-218x M and N Series
16-Bit Fixed-Point Digital Signal Processors

The ADSP-218x M and N series members offer low power (1.8V), low cost, and high performance 16-bit DSPs. All series members are pin and code compatible and are differentiated solely by the amount of on-chip SRAM. These feature combined with ADSP-21xx code compatibility provide a great deal of flexibility in the design decision.

Features

- 0.3mA/MIP@ 1.8V core supply on "N" series
- 0.5mA/MIP @ 2.5V core supply on "M" series
- 12.5 ns instruction cycle time (80 MIPS)[1]
- Up to 48K words program RAM and 56K words data words on chip
- I/O voltage support to 3.3V
- 16-bit bit internal DMA port
- 8 bit memory DMA
- Two double buffered serial ports (1 with TDM mode)
- I/O memory interface with 2048 locations
- 100-lead LQFP, 144-lead mini-BGA

Benefits

- Simple algebraic assembly language reduces development time and time to market
- Pin compatible packages mitigate product development risks
- 16-bit bit DMA port makes bus interfacing easier
- Code compatible with all 21xx derivatives ensures reuse of legacy code
- Large on chip memory eliminates the need for expensive SRAM
- 144-ball mini-BGA package provides for maximum space savings (10 mm x 10 mm)

Applications

- Consumer telephony
- Embedded speech processing
- POS terminals
- PBX
- Smart card readers
- Multi channel voice processing
- Industrial measurement control

[1] 13 ns on 'M' series

Model**	MHz	Memory Words PM/DM	Pin/Pkg	Price* (1000)
ADSP-2188NBST-320	80	48K/56K	100-LQFP	$26.00
ADSP-2188NBCA-320	80	48K/56K	144-MBGA	$28.00
ADSP-2189NBST-320	80	32K/48K	100-LQFP	$21.00
ADSP-2189NBCA-320	80	32K/48K	144-MBGA	$23.00
ADSP-2187NBST-320	80	32K/32K	100-LQFP	$17.00
ADSP-2187NBCA-320	80	32K/32K	144-MBGA	$19.00
ADSP-2185NBST-320	80	16K/16K	100-LQFP	$9.50
ADSP-2185NBCA-320	80	16K/16K	144-MBGA	$12.00
ADSP-2186NBST-320	80	8K/8K	100-LQFP	$7.25
ADSP-2186NBCA-320	80	8K/8K	144-MBGA	$9.25
ADSP-2184NBST-320	80	4K/4K	100-LQFP	$5.75
ADSP-2184NBCA-320	80	4K/4K	144-MBGA	$7.75
ADSP-2188MBST-266	66	48K/56K	100-LQFP	$28.00
ADSP-2188MBCA-266	66	48K/56K	144-MBGA	$30.00
ADSP-2189MBST-266	66	32K/48K	100-LQFP	$23.00
ADSP-2189MBCA-266	66	32K/48K	144-MBGA	$25.00
ADSP-2185MBST-266	66	16K/16K	100-LQFP	$10.00
ADSP-2185MBCA-266	66	16K/16K	144-MBGA	$12.00
ADSP-2186MBST-266	66	8K/8K	100-LQFP	$7.50
ADSP-2186MBCA-266	66	8K/8K	144-MBGA	$9.50
ADSP-2188NKST-320	80	48K/56K	100-LQFP	$26.00
ADSP-2188NKCA-320	80	48K/56K	144-MBGA	$28.00
ADSP-2189NKST-320	80	32K/48K	100-LQFP	$21.00
ADSP-2189NKCA-320	80	32K/48K	144-MBGA	$23.00
ADSP-2187NKST-320	80	32K/32K	100-LQFP	$17.00
ADSP-2187NKCA-320	80	32K/32K	144-MBGA	$19.00
ADSP-2185NKST-320	80	16K/16K	100-LQFP	$9.50
ADSP-2185NKCA-320	80	16K/16K	144-MBGA	$12.00
ADSP-2186NKST-320	80	8K/8K	100-LQFP	$7.25
ADSP-2186NKCA-320	80	8K/8K	144-MBGA	$9.25
ADSP-2184NKST-320	80	4K/4K	100-LQFP	$5.75
ADSP-2184NKCA-320	80	4K/4K	144-MBGA	$7.75
ADSP-2188MKST-300	75	48K/56K	100-LQFP	$28.00
ADSP-2188MKCA-300	75	48K/56K	144-MBGA	$30.00
ADSP-2189MKST-300	75	32K/48K	100-LQFP	$23.00
ADSP-2189MKCA-300	75	32K/48K	144-MBGA	$25.00
ADSP-2185MKST-300	75	16K/16K	100-LQFP	$10.00
ADSP-2185MKCA-300	75	16K/16K	144-MBGA	$11.50
ADSP-2186MKST-300	75	8K/8K	100-LQFP	$7.50
ADSP-2186MKCA-300	75	8K/8K	144-MBGA	$9.50

** N indicates operating voltage: 1.8V core/1.8-3.3V I/O
** M indicates operating voltage: 2.5V core/2.5-3.3V I/O
B = Industrial Temp (-40ºC to +85ºC ambient)
K = Commercial Temp (0ºC to +70ºC ambient)
* All pricing is budgetary – subject to change

ADSP-2199x Family
Mixed Signal DSPs

The ADSP-2199x family of mixed-signal DSPs provides a single-chip high-performance solution with signal processing and mixed-signal integration for both current and future embedded control and signal processing applications. These products combine the ADSP-219x code-compatible DSP core, multichannel, high-resolution analog/ digital conversion, the right mix of embedded control peripherals, and comprehensive development tools. A variety of memory sizes address emerging market requirements with power efficient and high-performance solutions.

Features

- 160 MHz, ADSP-219x DSP core
- 8-Channel, 14-Bit, 20 MSPS ADC
- On-chip voltage reference and power-on-reset
- Up to 32K words program memory RAM
- Up to 16K words data memory RAM
- External memory interface (to 1M Word)
- Embedded Control Peripherals
  - Three-phase PWM generation unit
  - Incremental encoder interface unit
  - Dual auxiliary PWM outputs
  - Watchdog timer
  - Three 32-Bit, general purpose timers
  - 16-Bit general purpose flag I/O port
  - Peripheral interrupt controller
  - Synchronous serial (SPORT) and SPI
  - Communications ports

Applications

- Industrial motor drives
- Un-interruptible power supplies
- Optical networking control
- Data acquisition systems
- Test and measurement systems
- Portable Instrumentation
- Intelligent sensors
- Robotic control

Benefits

- ADSP-219x core delivers highest performance mixed-signal DSP for control designs with up to 160 MIPS sustained performance
- Code compatible solution ensures investment protection with lower software cost
- State-of-the-art development tools
- Integrated single-chip pin-compatible solutions facilitate high-performance design with higher reliability, reduces development time with lower overall system cost
- External memory interface provides direct access from DSP to external memory for data or instruction
- Fabricated in high-speed, low power consumption, CMOS process

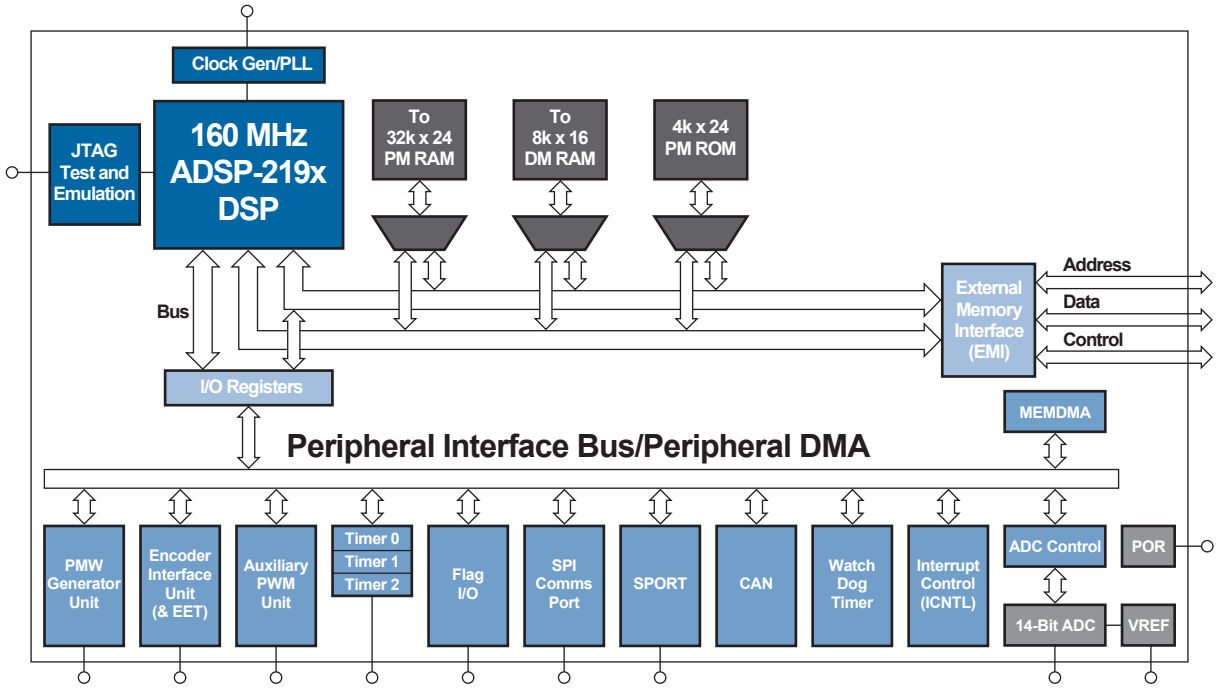
Mixed Signal DSP applications support can be obtained at mixedsignaldsp@analog.com. Users can also obtain additional support, free software upgrades, and sample code by visiting **www.analog.com/processors**.

ADSP-2199x Family
Mixed Signal DSPs

Model	MHz	Memory Words			Operating Voltage Core, I/O	Pin/Pkg	Price* (1000)
		DM RAM	PM RAM	PM ROM			
ADSP-21990BST	160	4K	4K	4K	2.5V/3.3V	176-LQFP	$19.25
ADSP-21990BBC	150	4K	4K	4K	2.5V/3.3V	196-MBGA	$20.30
ADSP-21991BST	160	8K	32K	4K	2.5V/3.3V	176-LQFP	$22.55
ADSP-21991BBC	150	8K	32K	4K	2.5V/3.3V	196-MBGA	$24.15
ADSP-21992BST	160	16K	32K	4K	2.5V/3.3V	176-LQFP	$24.75
ADSP-21992BBC	150	16K	32K	4K	2.5V/3.3V	196-MBGA	$26.35
ADSP-21992YST	100	16K	32K	4K	2.5V/3.3V	176-LQFP	$24.75
ADSP-21992YBC	150	16K	32K	4K	2.5V/3.3V	196-MBGA	$26.35

B = Industrial Temperature Range (-40ºC to +85ºC)
Y = Automotive Temperature Range (-40ºC to +125ºC)

Package: MBGA = Mini Ball Grid Array (15mm x 15 mm)
LQFP = Low-profile Quad Flat Pack (24mm x 24mm)
* All pricing is budgetary – subject to change



DSP Technical Training Workshops

Cut your time-to-market by getting up to speed fast. The DSP System Development and Programming workshops give you comprehensive hands-on training on Analog Devices DSPs. The workshops are geared towards people who have a working knowledge of microprocessors and want to learn how to use Analog Devices DSPs. These courses cover the DSP architecture, assembly language syntax, I/O interface, hardware and software development tools. Throughout the workshop, attendees learn how easy it is to use Analog Devices' DSPs from lecture sessions and hands-on exercises.

Locations and Schedules

Workshops are offered monthly in North America. Workshops are also offered in France, Germany, Italy, Scandinavia, UK and Spain. Workshop schedules and course details are available on the website at:

http://www.analog.com/processors

ADI Support for Universities

The ADI DSP University Program provides the next generation of engineers with DSP knowledge to help them compete in the industry of tomorrow.

The ADI DSP University Program offers:

- Complete DSP Software and Hardware Tools to set up a DSP LAB
- Teaching material to help design experiments
- Priority technical support to professors

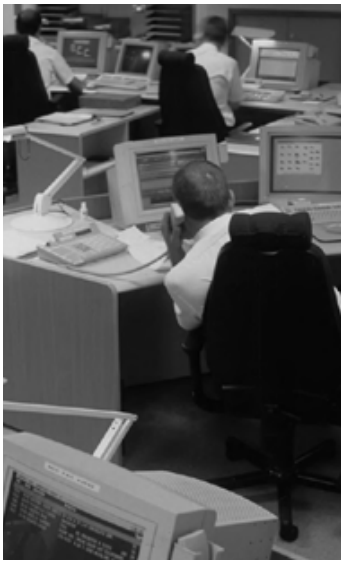
Analog Devices DSP technology is easy to teach:

- DSP architectures that are the simplest to program in the industry
- Simple instruction sets
- High levels of SRAM integration

Hundreds of universities in 59 countries use ADI DSPs for teaching and research.

To request a University discount or learn more, go to:

http://www.analog.com/dsp/university



Literature Guide

Title	Where to Order	Publication Number	Price
Blackfin Processor Data Sheets			
ADSP-BF531	www.analog.com/processors	Preliminary	NC
ADSP-BF532	www.analog.com/processors	Preliminary	NC
ADSP-BF533	www.analog.com/processors	Preliminary	NC
ADSP-BF535	www.analog.com/processors	Preliminary	NC
Blackfin Processor Publications			
ADSP-21535 Blackfin DSP Hardware Reference	www.analog.com/processors	82-000410-13	NC
Blackfin DSP Instruction Set Reference	www.analog.com/processors	82-000410-14	NC
Blackfin Processor Development Board and Emulator Publications			
ADSP-21535 EZ-KIT Lite Evaluation Kit Manual	www.analog.com/processors		NC
HPPCI-ICE Emulator Hardware User's Guide	www.analog.com/processors		
Apex-ICE™ USB Emulator Hardware Installation Guide	www.analog.com/processors		
VisualDSP++ for Blackfin Processors			
Complete Set of ADSP-BFxxx VisualDSP++ Manuals - includes the following:	From ADI Sales and Dist.	VDSP-BLKFN-MAN-FUL	$100.00
VisualDSP++ Getting Started Guide for Blackfin DSPs	www.analog.com/processors		NC
VisualDSP++ User's Guide for Blackfin DSPs	www.analog.com/processors		NC
VisualDSP++ C/C++ Compiler and Library Manual for Blackfin DSPs	www.analog.com/processors		NC
VisualDSP++ Assembler and Preprocessor Manual for Blackfin DSPs	www.analog.com/processors		NC
VisualDSP++ Linker and Utilities Manual for Blackfin DSPs	www.analog.com/processors		NC
VisualDSP++ Kernel (VDK) User's Guide (Second Revision)	www.analog.com/processors		NC
VisualDSP++ Installation Guide	www.analog.com/processors		NC
VisualDSP++ Component Software User's Guide	www.analog.com/processors		NC
ADSP-21xx and Mixed Signal DSP Data Sheets			
ADSP-2181	www.analog.com/processors		NC
ADSP-2183	www.analog.com/processors		NC
ADSP-2185M	www.analog.com/processors		NC
ADSP-2186M	www.analog.com/processors		NC
ADSP-2188M	www.analog.com/processors		NC
ADSP-2189M	www.analog.com/processors		NC
ADSP-218xN Series	www.analog.com/processors		NC
ADSP-2191M	www.analog.com/processors		NC
ADSP-2192	www.analog.com/processors		NC
ADSP-2195	www.analog.com/processors	Preliminary	NC
ADSP-2196	www.analog.com/processors	Preliminary	NC
ADSP-21990	www.analog.com/processors	Preliminary	NC
ADSP-21991	www.analog.com/processors	Preliminary	NC
ADSP-21992	www.analog.com/processors	Preliminary	NC
ADSP-21xx and Mixed Signal DSP Publications			
ADSP-2100 Family User's Manual	www.analog.com/processors		NC
ADSP-218x DSP Hardware Reference Manual	www.analog.com/processors	82-002010-01	NC
ADSP-218x DSP Instruction Set Reference	www.analog.com/processors	82-002000-01	NC
ADSP-219x/2191 DSP Hardware Reference Manual	www.analog.com/processors	82-000390-06	NC
ADSP-219x/2192 DSP Hardware Reference Manual	www.analog.com/processors	82-002001-01	NC
ADSP-219x DSP Instruction Set Reference	www.analog.com/processors	82-000390-07	NC
ADSP-2199x Mixed Signal DSP Hardware Reference Manual	www.analog.com/processors		NC
ADSP-21xx and Mixed Signal DSP Development Board and Emulator Publications			
ADSP-218x DSP family and ADSP-2191 EZ-KITLite Installation Procedure	www.analog.com/processors		NC
ADSP-2191 EZ-KIT Lite Evaluation Kit Manual	www.analog.com/processors		NC
ADSP-2181 EZ-KIT Lite Evaluation Kit Manual	www.analog.com/processors		NC
ADSP-2189M EZ-KIT Lite Evaluation Manual	www.analog.com/processors		NC
ADSP-21992 EZ-KIT Lite Evaluation Kit Manual	www.analog.com/processors		NC
ADSP-218X Family EZ-ICE® Hardware Installation Guide	www.analog.com/processors		NC
HPPCI-ICE Emulator Hardware User's Guide	www.analog.com/processors		NC
Apex-ICE™ USB Emulator Hardware Installation Guide	www.analog.com/processors		NC
VisualDSP++ for ADSP-21xx and Mixed Signal DSPs			
Complete Set of ADSP-21xx VisualDSP++ Manuals - includes the following:	From ADI Sales and Dist.	VDSP-21XX-MAN-FULL	$100.00
VisualDSP++ Getting Started Guide for ADSP-21xx DSPs	www.analog.com/processors		NC
VisualDSP++ User's Guide for ADSP-21xx DSPs	www.analog.com/processors		NC
VisualDSP++ C Compiler and Library Manual for ADSP-218x DSPs	www.analog.com/processors		NC
VisualDSP++ C/C++ Compiler and Library Manual for ADSP-219x DSPs	www.analog.com/processors		NC
VisualDSP++ Assembler and Preprocessor Manual for ADSP-218x DSPs	www.analog.com/processors		NC
VisualDSP++ Assembler and Preprocessor Manual for ADSP-219x DSPs	www.analog.com/processors		NC
VisualDSP++ Linker and Utilities Manual for ADSP-21xx DSPs	www.analog.com/processors		NC
VisualDSP++ Kernel (VDK) User's Guide VisualDSP++ Installation Guide	www.analog.com/processors		NC
VisualDSP++ Component Software User's Guide	www.analog.com/processors		NC

Literature Guide

Title	Where to Order	Publication Number	Price
TigerSHARC Processor Data Sheets			
ADSP-TS101S	www.analog.com/processors		NC
TigerSHARC Processor Publications			
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VisualDSP++ Installation Guide	www.analog.com/processors		NC

* NC = No charge

** Data Sheets and Manuals can also be downloaded from the ADI DSP website

ADI Power Management Guide

			Recommended ADI Power Management Devices for Maximum DSP Core and I/O Currents			
			1 DSP		2 or More DSPs	
DSP Family	DSP Supply Voltage (nominal)	Max Suppy Current	LDO	DC/DC Switching Regulator or Controller	LDO	DC/DC Switching Regulator or Controller
ADSP-TSxxx TigerSHARC Platform						
	1.2Vcore	1.6 W	ADP3170	ADP3170	ADP3170	ADP3170
ADSP-TS101S	3.3V I/O	137 mA	ADP3170	ADP3170	ADP3170	ADP3170
ADSP-21xxx SHARC Platform						
	3.3Vcore	275 mA	ADP3333	ADP3088	ADP3338	ADP3088
ADSP-21065L	3.3V I/O	21 mA	ADP3309	ADP3088	ADP3309	ADP3088
	2.5Vcore	875 mA	ADP3338/9	ADP3088	-	-
ADSP-21160M	3.3V I/O	41 mA	ADP3309	ADP3088	ADP3309	ADP3088
	1.8V core	875 mA	ADP3338/9	ADP3088	-	-
ADSP-21160N	3.3V I/O	72 mA	ADP3309	ADP3088	ADP3330	ADP3088
	1.8V core	550 mA	ADP3338	ADP3088	-	ADP3050
ADSP-21161N	3.3V I/O	56 mA	ADP3309	ADP3088	ADP3330	ADP3088
ADSP-21xx Platform						
	1.8V core	25 mA	ADP3331	ADP3088	ADP3331	ADP3088
ADSP-2184N	3.3V I/O	14 mA	ADP3309	ADP3088	ADP3309	ADP3088
	2.5V core	38 mA	ADP3309	ADP3088	ADP3309	ADP3088
ADSP-2185M	3.3V I/O	12 mA	ADP3300	ADP3088	ADP3309	ADP3088
	1.8V core	25 mA	ADP3331	ADP3088	ADP3331	ADP3088
ADSP-2185N	3.3V I/O	14 mA	ADP3300	ADP3088	ADP3309	ADP3088
	2.5Vcore	38 mA	ADP3309	ADP3088	ADP3309	ADP3088
ADSP-2186M	3.3V I/O	12 mA	ADP3300	ADP3088	ADP3309	ADP3088
	1.8Vcore	25 mA	ADP3331	ADP3088	ADP3331	ADP3088
ADSP-2186N	3.3V I/O	14 mA	ADP3330	ADP3088	ADP3309	ADP3088
	1.8Vcore	26 mA	ADP3331	ADP3088	ADP3331	ADP3088
ADSP-2187N	3.3V I/O	14 mA	ADP3300	ADP3088	ADP3309	ADP3088
	2.5Vcore	44 mA	ADP3309	ADP3088	ADP3309	ADP3088
ADSP-2188M	3.3V I/O	12 mA	ADP3300	ADP3088	ADP3309	ADP3088
	1.8Vcore	25 mA	ADP3331	ADP3088	ADP3331	ADP3088
ADSP-2188N	3.3V I/O	14 mA	ADP3300	ADP3088	ADP3309	ADP3088
	2.5Vcore	32 mA	ADP3309	ADP3088	ADP3331	ADP3088
ADSP-2189M	3.3V I/O	15mA	ADP3300	ADP3088	ADP3309	ADP3088
	1.8Vcore	26 mA	ADP3331	ADP3088	ADP3331	ADP3088
ADSP-2189N	3.3V I/O	14 mA	ADP3330	ADP3088	ADP3309	ADP3088
	2.5V core	184 mA	ADP3330	ADP3088	ADP3335	ADP3088
ADSP-2191M	3.3V I/O	14 mA	ADP3300	ADP3088	ADP3309	ADP3088
	2.5V core	184 mA	ADP3330	ADP3088	ADP3335	ADP3088
ADSP-2195M	3.3V I/O	14 mA	ADP3300	ADP3088	ADP3309	ADP3088
	2.5V core	184 mA	ADP3330	ADP3088	ADP3335	ADP3088
ADSP-2196M	3.3V I/O	14 mA	ADP3300	ADP3088	ADP3309	ADP3088

ADI DSP-Supervisory Guide

ADI DSP Family	DSP Supply Voltage	Reset Generators Only	With Open Drain Output		With Manual Reset		With Watchdog
ADSP-BF53x Blackfin® Platform		**Recommended ADI Supervisory Devices**					
	0.7-1.2V	-	-	-	-	-	-
ADSP-BF531	3.3V I/O	ADM809/10(R/S/T)	ADM1816/8*	ADM6315	ADM811R/S/T	ADM6315	ADM706R/S/T
	0.7-1.2V	-	-	-	-	-	-
ADSP-BF532	3.3V I/O	ADM809/10(R/S/T)	ADM1816/8*	ADM6315	ADM811R/S/T	ADM6315	ADM706R/S/T
	0.7-1.2V	-	-	-	-	-	-
ADSP-BF533	3.3V I/O	ADM809/10(R/S/T)	ADM1816/8*	ADM6315	ADM811R/S/T	ADM6315	ADM706R/S/T
	1.0-1.6V	-	-	-	-	-	-
ADSP-BF535	3.3V I/O	ADM809/10(R/S/T)	ADM1816/8*	ADM6315	ADM811R/S/T	ADM6315	ADM706R/S/T
ADSP-TSxxx TigerSHARC® Platform		**Recommended ADI Supervisory Devices**					
	1.2V core	-	-	-	-	-	-
ADSP-TS101S	3.3V I/O	ADM809/10(R/S/T)	ADM1816/8*	ADM6315	ADM811R/S/T	ADM6315	ADM706R/S/T
ADSP-21xxx SHARC® Platform		**Recommended ADI Supervisory Devices**					
	3.3Vcore	ADM809/10(R/S/T)	ADM1816/8*	ADM6315	ADM811R/S/T	ADM6315	ADM706R/S/T
ADSP-21065L	3.3V I/O	ADM809/10(R/S/T)	ADM1816/8*	ADM6315	ADM811R/S/T	ADM6315	ADM706R/S/T
	2.5Vcore	ADM809Z	ADM1818-R22/R23*	-	ADM811Z	-	-
ADSP-21160M	3.3V I/O	ADM809/10(R/S/T)	ADM1816/8*	ADM6315	ADM811R/S/T	ADM6315	ADM706R/S/T
	1.8V core	-	-	-	-	-	-
ADSP-21160N	3.3V I/O	ADM809/10(R/S/T)	ADM1816/8*	ADM6315	ADM811R/S/T	ADM6315	ADM706R/S/T
	1.8V core	-	-	-	-	-	-
ADSP-21161N	3.3V I/O	ADM809/10(R/S/T)	ADM1816/8*	ADM6315	ADM811R/S/T	ADM6315	ADM706R/S/T
ADSP-21xx Platform		**Recommended ADI Supervisory Devices**					
	1.8V core	-	-	-	-	-	-
ADSP-2184N	3.3V I/O	ADM809/10(R/S/T)	ADM1816/8*	ADM6315	ADM811R/S/T	ADM6315	ADM706R/S/T
	2.5V core	ADM809Z	ADM1818-R22/R23*	-	ADM811Z	-	-
ADSP-2185M	3.3V I/O	ADM809/10(R/S/T)	ADM1816/8*	ADM6315	ADM811R/S/T	ADM6315	ADM706R/S/T
	1.8V core	-	-	-	-	-	-
ADSP-2185N	3.3V I/O	ADM809/10(R/S/T)	ADM1816/8*	ADM6315	ADM811R/S/T	ADM6315	ADM706R/S/T
	2.5Vcore	ADM809Z	ADM1818-R22/R23*	-	ADM811Z	-	-
ADSP-2186M	3.3V I/O	ADM809/10(R/S/T)	ADM1816/8*	ADM6315	ADM811R/S/T	ADM6315	ADM706R/S/T
	1.8Vcore	-	-	-	-	-	-
ADSP-2186N	3.3V I/O	ADM809/10(R/S/T)	ADM1816/8*	ADM6315	ADM811R/S/T	ADM6315	ADM706R/S/T
	1.8Vcore	-	-	-	-	-	-
ADSP-2187N	3.3V I/O	ADM809/10(R/S/T)	ADM1816/8*	ADM6315	ADM811R/S/T	ADM6315	ADM706R/S/T
	2.5Vcore	ADM809Z	ADM1818-R22/R23*	-	ADM811Z	-	-
ADSP-2188M	3.3V I/O	ADM809/10(R/S/T)	ADM1816/8*	ADM6315	ADM811R/S/T	ADM6315	ADM706R/S/T
	1.8Vcore	-	-	-	-	-	-
ADSP-2188N	3.3V I/O	ADM809/10(R/S/T)	ADM1816/8*	ADM6315	ADM811R/S/T	ADM6315	ADM706R/S/T
	2.5Vcore	ADM809Z	ADM1818-R22/R23*	-	ADM811Z	-	-
ADSP-2189M	3.3V I/O	ADM809/10(R/S/T)	ADM1816/8*	ADM6315	ADM811R/S/T	ADM6315	ADM706R/S/T
	1.8Vcore	-	-	-	-	-	-
ADSP-2189N	3.3V I/O	ADM809/10(R/S/T)	ADM1816/8*	ADM6315	ADM811R/S/T	ADM6315	ADM706R/S/T
	2.5V core	ADM809Z	ADM1818-R22/R23*	-	ADM811Z	-	-
ADSP-2191M	3.3V I/O	ADM809/10(R/S/T)	ADM1816/8*	ADM6315	ADM811R/S/T	ADM6315	ADM706R/S/T
	2.5V core	ADM809Z	ADM1818-R22/R23*	-	ADM811Z	-	-
ADSP-2195M	3.3V I/O	ADM809/10(R/S/T)	ADM1816/8*	ADM6315	ADM811R/S/T	ADM6315	ADM706R/S/T
	2.5V core	ADM809Z	ADM1818-R22/R23*	-	ADM811Z	-	-
ADSP-2196M	3.3V I/O	ADM809/10(R/S/T)	ADM1816/8*	ADM6315	ADM811R/S/T	ADM6315	ADM706R/S/T

* Weak internal Pull-up which can be overdriven by external resistor

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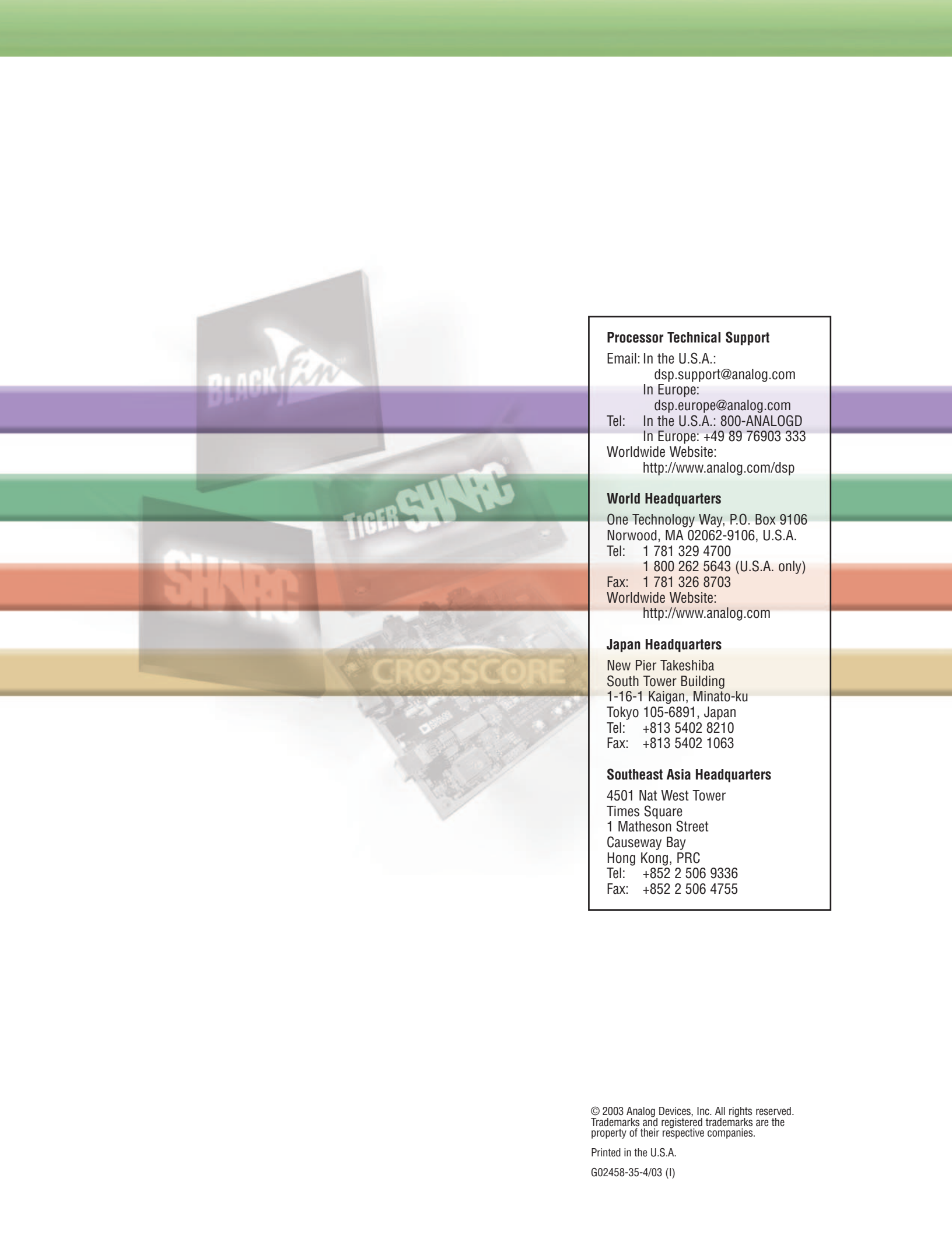

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